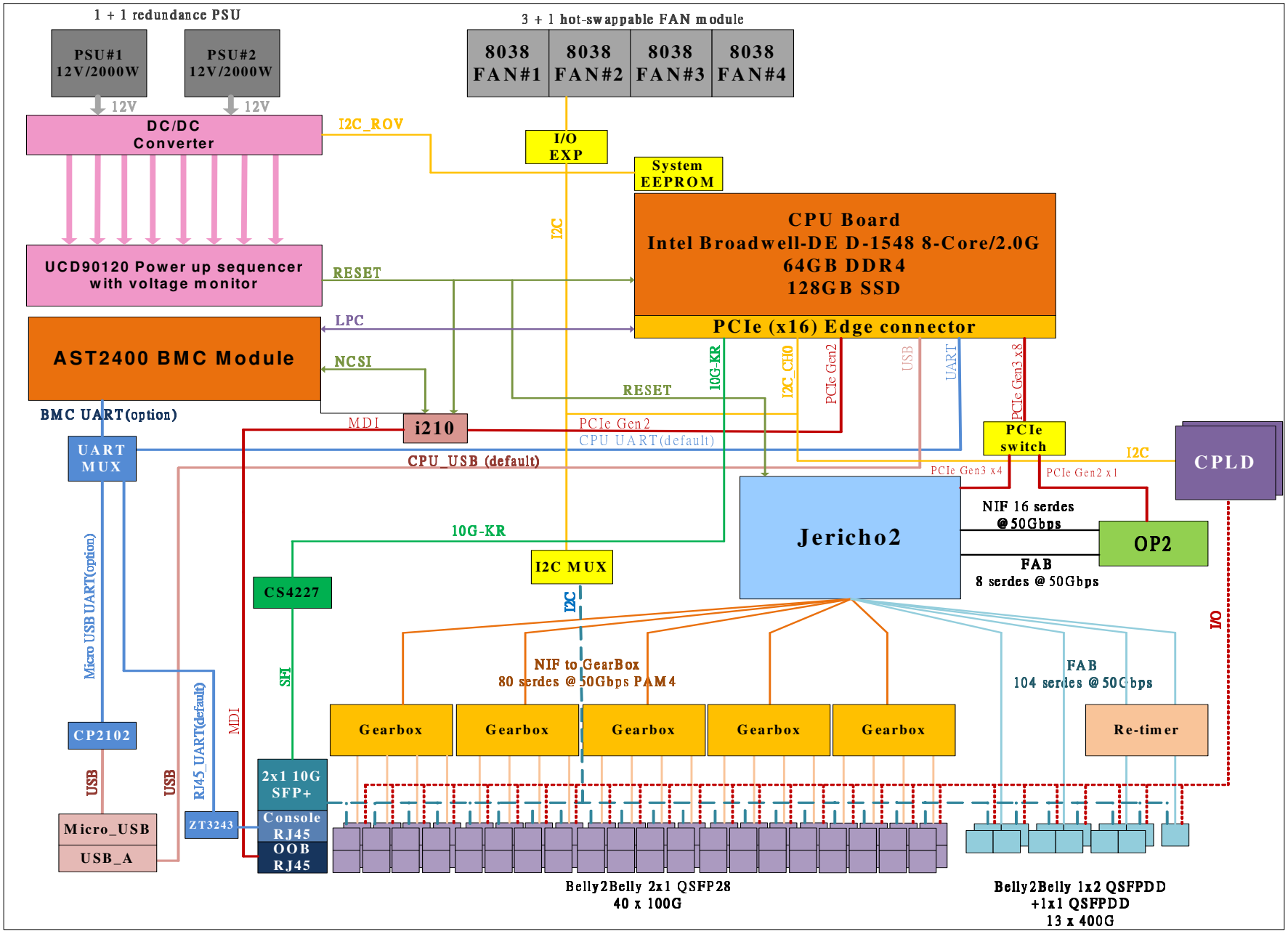
001_Title Page
002_SYSTEM BLOCK DIAGRAM
003_Jericho2_Fabric_Serdes
004_Jericho2_NIF_Serdes
005_Jericho2_Management
006_Jericho2_Control
007_Jericho2_PUC_Test_DRAM_Test
008_Jericho2_Clock
009_Jericho2_VDDC_VDDO_PCIE_PLL
010_Jericho2_VDDC_Caps
011_Jericho2_TRVDD
012_Jericho2_TRVDD_Caps
013_Jericho2_PVDD_TVDD1P2V_Caps
014_Jericho2_DRAM_Power
015_Jericho2_GND1
016_Jericho2_GND2
017_Jericho2_GND3
018_Gearbox Host_Line I/F_01~02
019_Gearbox Host_Line I/F_03~04
020_Gearbox Host_Line I/F_05~06
021_Gearbox Host_Line I/F_07~08
022_Gearbox Host_Line I/F_09~10
023_Gearbox RESET_MDIO_JTAG_01
024_Gearbox RESET_MDIO_JTAG_02
025_Gearbox RESET_MDIO_JTAG_03
026_Gearbox RESET_MDIO_JTAG_04
027_Gearbox RESET_MDIO_JTAG_05
028_Gearbox RESET_MDIO_JTAG_06
029_Gearbox RESET_MDIO_JTAG_07
030_Gearbox RESET_MDIO_JTAG_08
031_Gearbox RESET_MDIO_JTAG_09
032_Gearbox RESET_MDIO_JTAG_10
033_Gearbox Power_01
034_Gearbox Power_02
035_Gearbox Power_03
036_Gearbox Power_04
037_Gearbox Power_05
038_Gearbox Power_06
039_Gearbox Power_07
040_Gearbox Power_08
041_Gearbox Power_09
042_Gearbox Power_10
043_Gearbox GND_01~02
044_Gearbox GND_03~04
045_Gearbox GND_05~06
046_Gearbox GND_07~08
047_Gearbox GND_09~10
048_OP2_JTAG_MISC
049_OP2_Serdes
050_OP2_Reset_Clock_PCIE
051_OP2_Power_VDD
052_OP2_Power_VDDH_HVA_LVA_LVD
053_OP2_GND
054_QSFP28 Port 01~04
055_QSFP28 Port 05~08
056_QSFP28 Port 09~12
057_QSFP28 Port 13~16
058_QSFP28 Port 17~20
059_QSFP28 Port 21~24
060_QSFP28 Port 25~28
061_QSFP28 Port 29~32
062_QSFP28 Port 33~36
063_QSFP28 Port 37~40
064_QSFPDD_FAB Port 1 & 3
065_QSFPDD_FAB Port 2 & 4
066_QSFPDD_FAB Port 5 & 7
067_QSFPDD_FAB Port 6 & 8
068_QSFPDD_FAB Port 9 & 11
069_QSFPDD_FAB Port 10 & 12
070_QSFPDD_FAB Port 13
071_CLOCK_1
072_CLOCK_2
073_IEEE 1588
074_LED CIRCUIT
075_2X1SFP+ Connector
076_I2C SWITCH_CPLD/QSFP_0
077_I2C SWITCH_CPLD/QSFP_1
078_CPLD1 10M08DAU324C8G-1
079_CPLD1 10M08DAU324C8G-2
080_CPLD2 10M04DAU324C8G-1
081_CPLD2 10M04DAU324C8G-2
082_CPLD3 10M04DAU324C8G-1
083_CPLD3 10M04DAU324C8G-2
084_CPLD4 10M04DAU324C8G-1
085_CPLD4 10M04DAU324C8G-2
086_CPLD5 10M04DAU324C8G-1
087_CPLD5 10M04DAU324C8G-2
088_I2C DIAGRAM
089_I2C_SYSTEM
090_SCREW
091_SWITCH INT
092_PCIE CONNECTOR_0
093_PCIE CONNECTOR_1
094_CS4227_RESET_CLK_JTAG
095_CS4227_PHY
096_CS4227_Power
097_PCIE SW SerDes
098_PCIE SW MISC
099_PCIE SW Power & GND
100_SYSTEM LED
101_FAN CONNECTOR
102_POWER CONNECTOR
103_UCD90120A
104_BMC SOCKET0
105_BMC SOCKET1
106_HWM
107_ETH CONTROLLER WGI210AT
108_CONSOLE & OOB & USB
109_PUSH BUTTON & MICRO USB
110_BCM81358_PHY1_A
111_BCM81358_PHY1_B
112_BCM81358_PHY2_A
113_BCM81358_PHY2_B
114_BCM81358_PHY3_A
115_BCM81358_PHY3_B
116_BCM81358_PHY4_A
117_BCM81358_PHY4_B
118_BCM81358_PHY5_A
119_BCM81358_PHY5_B
120_SYSTEM PWR Sequence
121_12V to 5V
122_12V to 3V3/120A_NCP81233
123_12V to 3V3/120A_1-3
124_12V to 3V3/120A_4-6
125_5V to 3V3_CLK
126_3V3 to 2.5V/1.2A
127_3V3 to 1V8/3A
128_12V to AVS_0.8V/110A
129_12V to 1V2_1/12A
130_12V to 1V2_2/11A
131_12V to 1V2_3/5A
132_3V3 to 0.9V/1A
133_3V3 to 0V88/4A
134_12V to 0.85V/150A_NCP81233
135_12V to 0.85V/150A_1-4
136_12V to 0.85V/150A_5-6
137_12V to 0V8/127A_NCP81233
138_12V to 0V8/97A_1-6
139_3V3 to 1V8_PHY/3A
140_12V to ROV/438A_NCP81233
141_12V to ROV/438A_1-4
142_12V to ROV/438A_5-8
143_12V to ROV/438A_9-12
144_3V3 to 3V3_I2C/FAN
145_Coupon Impendence Test
146_12V to 0V8_Retimer/9.9A_1-3
147_12V to 0V8_Retimer/9.9A_4-5
148_12V to 0.85V_VDDM/9A
149_12V to 0.9V_PEX/12A
150_3V3 to 0V8_VDDSL/0.75A
151_CPLD POWER
152_12V to 0V8_MAC/62A_NCP81233

<Core Design>

UfiSpace Co., Ltd.

Title
001_Title Page

Document Number: PCB P/N: T99O114T00	Sheet 1 of 152	Rev 015

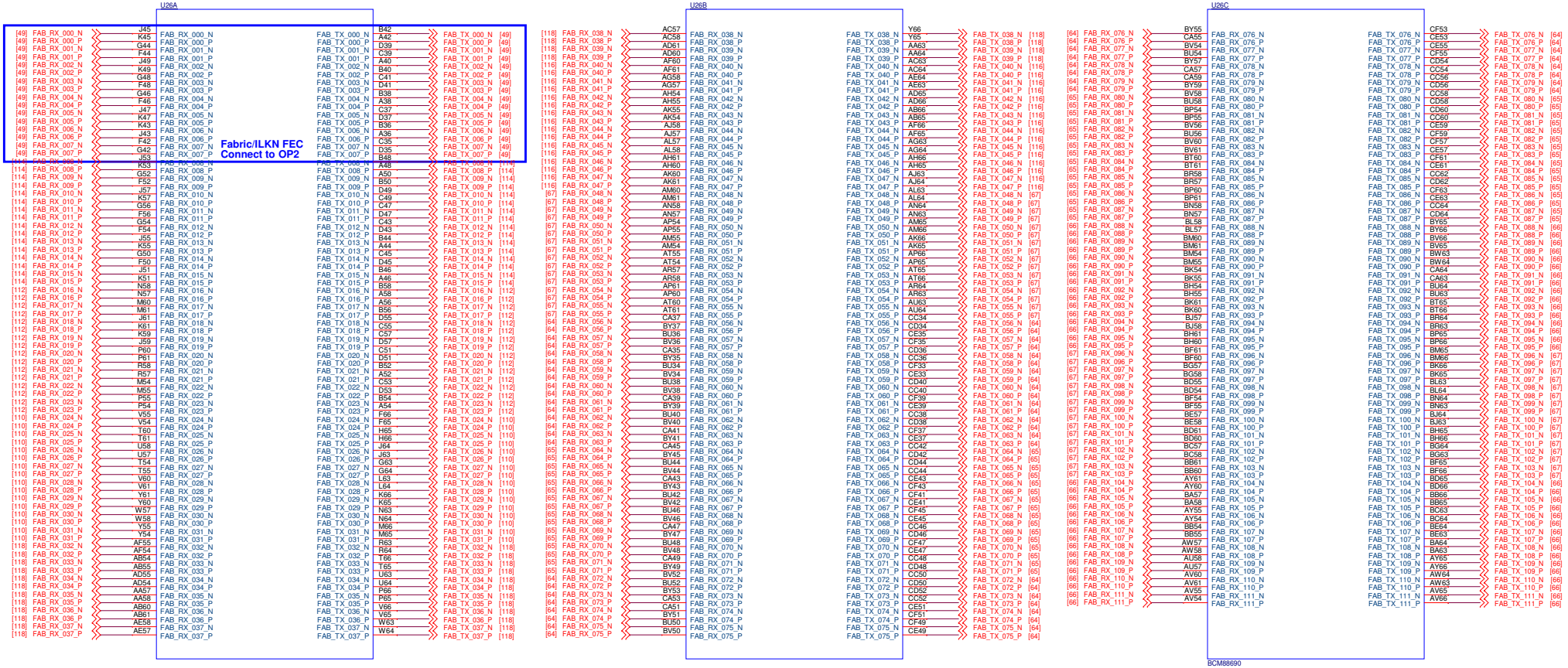


<Core Design>

UfiSpace Co., Ltd.

Title: 002_SYSTEM BLOCK DIAGRAM

Document Number: PCB P/N: T99O114T00	Sheet 2 of 152	Rev 015

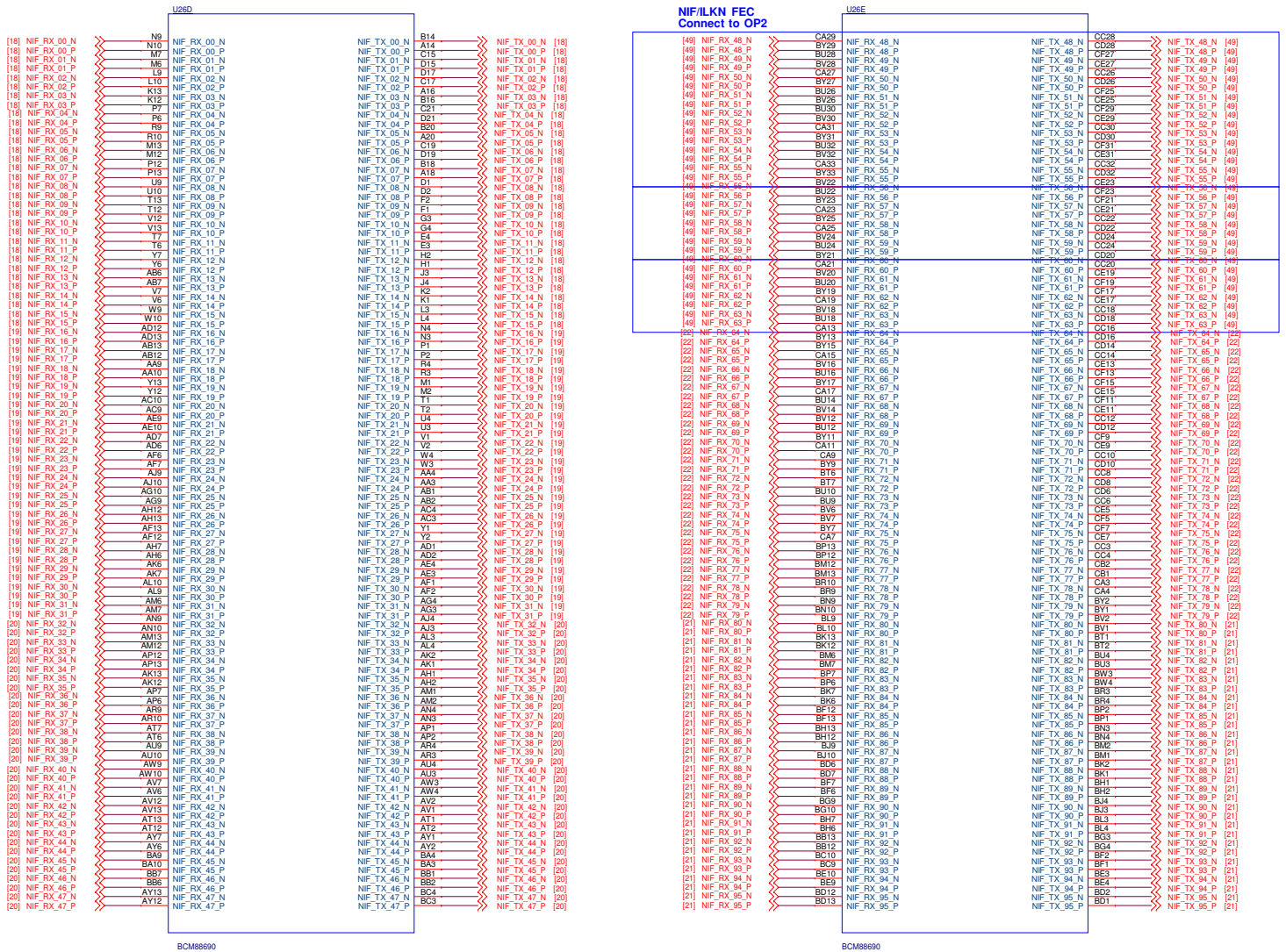


<Core Design>

UfiSpace Co., Ltd.

Title: 003_Jericho2_Fabric_Serdes

Document Number: T99O114T00 | Sheet 3 of 152 | Rev 015



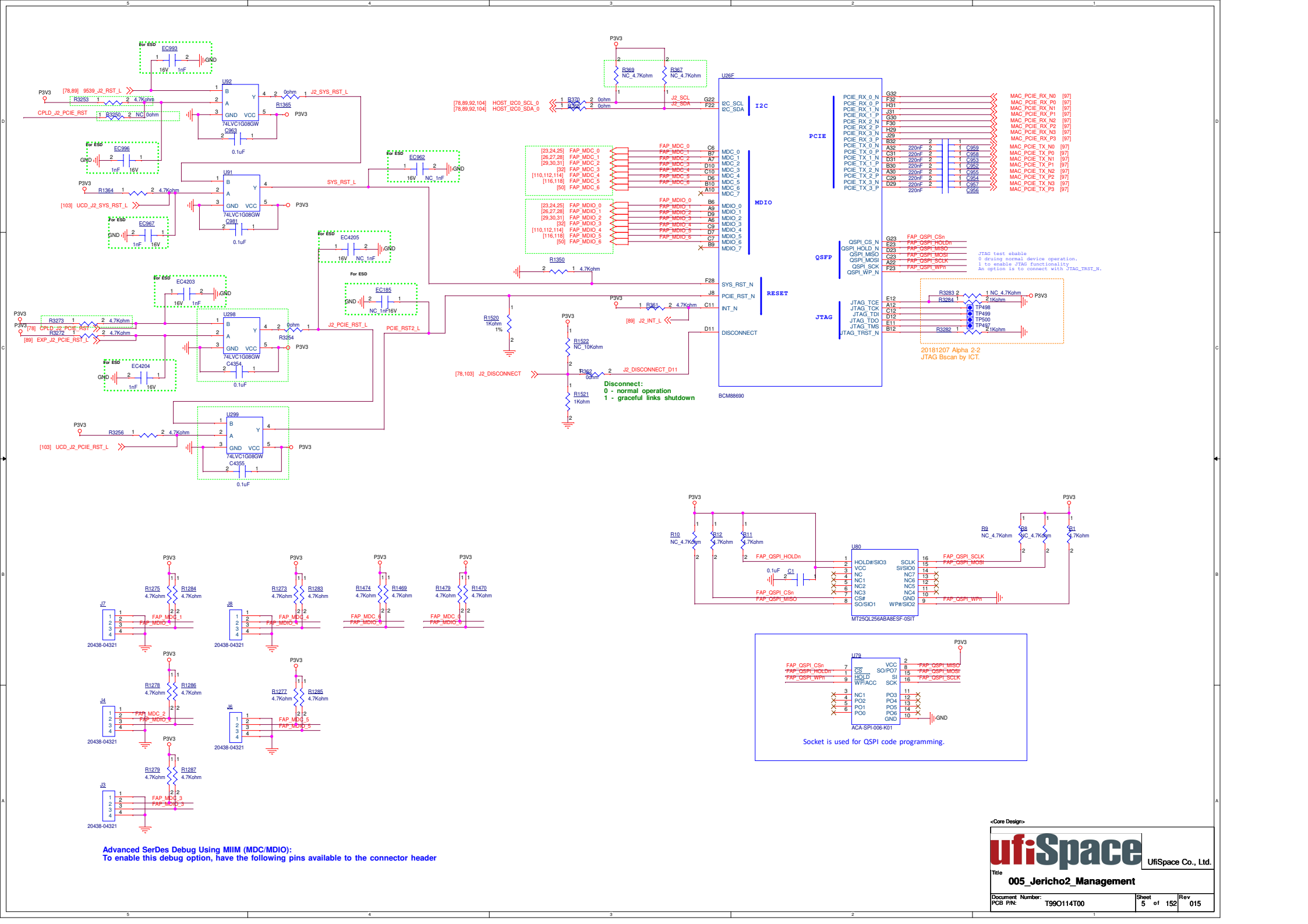
<Core Design>

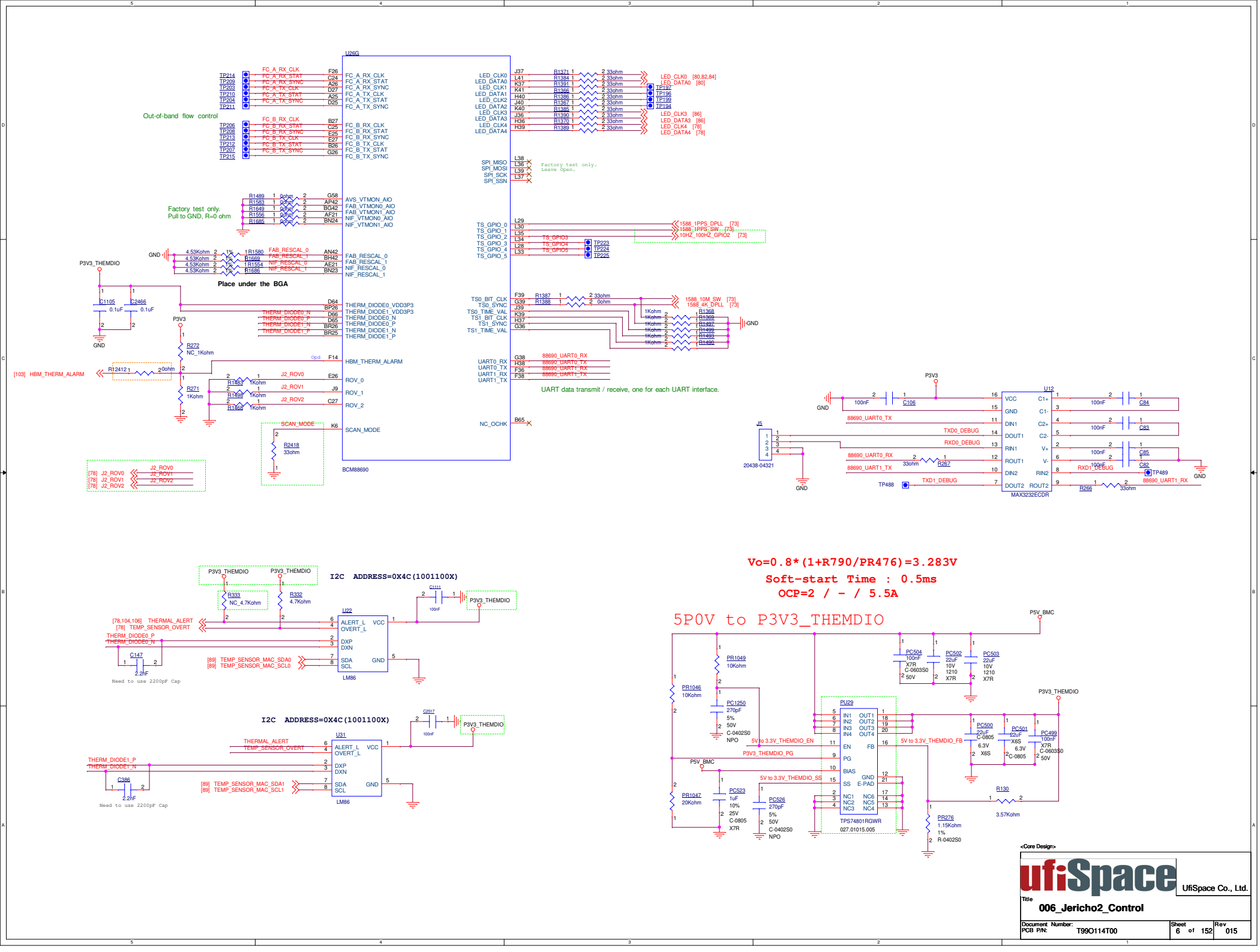
UfiSpace Co., Ltd.

Title

004_Jericho2_NIF_Serdes

Document Number: PCB P/N:	Sheet	Rev
T99O114T00	4 of 152	015


U26F
BCM88690
I2C
PCIE
MDIO
QSFP
RESET
JTAG
DISCONNECT
Disconnect:
0 - normal operation
1 - graceful links shutdown
JTAG test ebable
0 druing normal device operation.
1 to enable JTAG functionality
An option is to connect with JTAG_TRST_N.
20181207 Alpha 2-2
JTAG Bscan by ICT.
U80
MT25QL256ABA8ESF-0SIT
U79
ACA-SPI-006-K01
Socket is used for QSPI code programming.
Advanced SerDes Debug Using MIIM (MDC/MDIO):
To enable this debug option, have the following pins available to the connector header
ufiSpace
UfiSpace Co., Ltd.
Title
005_Jericho2_Management
Document Number:
PCB P/N: T99O114T00
Sheet 5 of 152
Rev 015



<Core Design>
UfiSpace Co., Ltd.

Title
006_Jericho2_Control

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	6 of 152	015

Factory test only.
Required connectivity:
[22:17] and [14:13] connected to GND.
Other FTEST pins should be left open.

U26H

U26I

BCM88690

Table 21: Power-Up Configuration Signal Description

PUC	Function	Description
PUC_[9:0]	CORE_PLL_N_DIV[9:0]	Set to 240 (PUC[9:0] = 0x0F0)
PUC_[18:10]	CORE_PLL_M_DIV[8:0]	Set to 6 (PUC[19:0] = 0x018F0)
PUC_[19]	Factory test.	Set to 0
PUC_[21:20]	I2C_SA[1:0]	Device I2C (BSC) slave address LSB. When the I2C (BSC) interface is used, the device physical address is made up of the following 7 bits: ■ [A6, A5, A4, A3, A2] fixed as 0x10001 ■ [A1, A0] set according to [PUC_21, PUC_20] Available addresses are 0x44, 0x45, 0x46, and 0x47.
PUC_[25:22]	Factory test.	Set to 0x0
PUC_[26]	PCIE_GSPI_ENABLE	Set to 1.
PUC_[29:27]	Factory test.	Set to 0x0

OP3V3

J18A

J18B

J18C

J18D

J18E

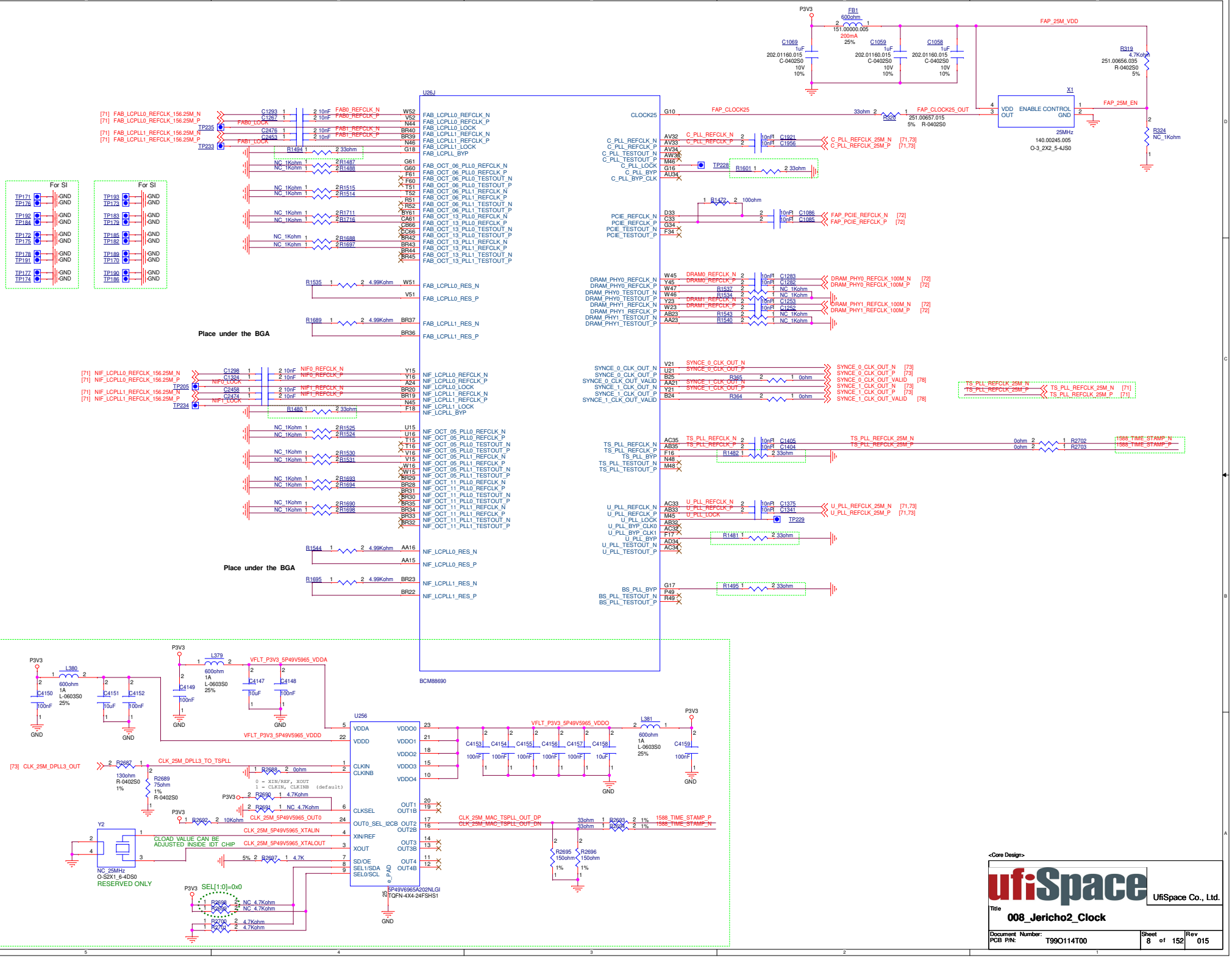
SEAF-15-05.0-S-10-2-A-K-TR

<Core Design>

UfiSpace Co., Ltd.

Title: 007_Jericho2_PUC_Test_DRAM_Test

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	7 of 152	015


U26J
BCM88690
Place under the BGA
Place under the BGA
For SI
For SI
U256
6P49V6965A202NLGI
TQFN-4X4-24FSHS1
FAP_25M_VDD
FAP_25M_EN
FAP_CLOCK25
FAP_CLOCK25_OUT
X1
ENABLE CONTROL
25MHz
140.00245.005
O-3_2X2_5-4JS0
C_PLL_REFCLK_25M_N [71,73]
C_PLL_REFCLK_25M_P [71,73]
FAP_PCIE_REFCLK_N [72]
FAP_PCIE_REFCLK_P [72]
DRAM_PHY0_REFCLK_100M_N [72]
DRAM_PHY0_REFCLK_100M_P [72]
DRAM_PHY1_REFCLK_100M_N [72]
DRAM_PHY1_REFCLK_100M_P [72]
SYNCE_0_CLK_OUT_N [73]
SYNCE_0_CLK_OUT_P [73]
SYNCE_0_CLK_OUT_VALID [78]
SYNCE_1_CLK_OUT_N [73]
SYNCE_1_CLK_OUT_P [73]
SYNCE_1_CLK_OUT_VALID [78]
TS_PLL_REFCLK_25M_N [71]
TS_PLL_REFCLK_25M_P [71]
1588_TIME_STAMP_N
1588_TIME_STAMP_P
U_PLL_REFCLK_25M_N [71,73]
U_PLL_REFCLK_25M_P [71,73]
BS_PLL_BYP
CLK_25M_DPLL3_TO_TSPLL
CLK_25M_MAC_TSPLL_OUT_DP
CLK_25M_MAC_TSPLL_OUT_DN
CLK_25M_5P49V5965_XTALIN
CLK_25M_5P49V5965_XTALOUT
CLOAD VALUE CAN BE ADJUSTED INSIDE IDT CHIP
RESERVED ONLY
NC_25MHz
O-S2X1_6-4DS0
SEL[1:0]=0x0
VFLT_P3V3_5P49V5965_VDDA
VFLT_P3V3_5P49V5965_VDDD
VFLT_P3V3_5P49V5965_VDDO
[73] CLK_25M_DPLL3_OUT
0 = XIN/REF, XOUT
1 = CLKIN, CLKINB (default)
<Core Design>
UfiSpace Co., Ltd.
Title
008_Jericho2_Clock
Document Number:
PCB P/N:
T99O114T00
Sheet 8 of 152
Rev 015

355A

U26K

ROV_CORE

AB44	VDDC_AB44	AR33	VDDC_AR33
AC21	VDDC_AC21	AR35	VDDC_AR35
AC23	VDDC_AC23	AR37	VDDC_AR37
AC45	VDDC_AC45	AR39	VDDC_AR39
AD22	VDDC_AD22	AT22	VDDC_AT22
AD24	VDDC_AD24	AT24	VDDC_AT24
AD44	VDDC_AD44	AT26	VDDC_AT26
AE27	VDDC_AE27	AT28	VDDC_AT28
AE29	VDDC_AE29	AT30	VDDC_AT30
AE31	VDDC_AE31	AT32	VDDC_AT32
AE37	VDDC_AE37	AT34	VDDC_AT34
AE39	VDDC_AE39	AT36	VDDC_AT36
AE41	VDDC_AE41	AT38	VDDC_AT38
AE43	VDDC_AE43	AT40	VDDC_AT40
AE45	VDDC_AE45	AU21	VDDC_AU21
AF26	VDDC_AF26	AU23	VDDC_AU23
AF28	VDDC_AF28	AU25	VDDC_AU25
AF30	VDDC_AF30	AU27	VDDC_AU27
AF32	VDDC_AF32	AU29	VDDC_AU29
AF34	VDDC_AF34	AU31	VDDC_AU31
AF36	VDDC_AF36	AU35	VDDC_AU35
AF38	VDDC_AF38	AU37	VDDC_AU37
AF40	VDDC_AF40	AU39	VDDC_AU39
AF42	VDDC_AF42	AV22	VDDC_AV22
AF44	VDDC_AF44	AV24	VDDC_AV24
AG27	VDDC_AG27	AV26	VDDC_AV26
AG29	VDDC_AG29	AV28	VDDC_AV28
AG31	VDDC_AG31	AV30	VDDC_AV30
AG33	VDDC_AG33	AV36	VDDC_AV36
AG35	VDDC_AG35	AV38	VDDC_AV38
AG37	VDDC_AG37	AV40	VDDC_AV40
AG39	VDDC_AG39	AW21	VDDC_AW21
AG41	VDDC_AG41	AW23	VDDC_AW23
AG43	VDDC_AG43	AW25	VDDC_AW25
AG45	VDDC_AG45	AW29	VDDC_AW29
AH26	VDDC_AH26	AW31	VDDC_AW31
AH28	VDDC_AH28	AW35	VDDC_AW35
AH30	VDDC_AH30	AW37	VDDC_AW37
AH32	VDDC_AH32	AW39	VDDC_AW39
AH34	VDDC_AH34	AY22	VDDC_AY22
AH36	VDDC_AH36	AY24	VDDC_AY24
AH38	VDDC_AH38	AY26	VDDC_AY26
AH40	VDDC_AH40	AY28	VDDC_AY28
AH42	VDDC_AH42	AY30	VDDC_AY30
AH44	VDDC_AH44	AY32	VDDC_AY32
AJ25	VDDC_AJ25	AY34	VDDC_AY34
AJ27	VDDC_AJ27	AY36	VDDC_AY36
AJ29	VDDC_AJ29	AY38	VDDC_AY38
AJ31	VDDC_AJ31	AY40	VDDC_AY40
AJ33	VDDC_AJ33	BA21	VDDC_BA21
AJ35	VDDC_AJ35	BA23	VDDC_BA23
AJ37	VDDC_AJ37	BA25	VDDC_BA25
AJ39	VDDC_AJ39	BA27	VDDC_BA27
AJ41	VDDC_AJ41	BA29	VDDC_BA29
AK26	VDDC_AK26	BA31	VDDC_BA31
AK28	VDDC_AK28	BA33	VDDC_BA33
AK30	VDDC_AK30	BA35	VDDC_BA35
AK32	VDDC_AK32	BA37	VDDC_BA37
AK34	VDDC_AK34	BA39	VDDC_BA39
AK36	VDDC_AK36	BB22	VDDC_BB22
AK38	VDDC_AK38	BB24	VDDC_BB24
AK40	VDDC_AK40	BB26	VDDC_BB26
AL25	VDDC_AL25	BB28	VDDC_BB28
AL27	VDDC_AL27	BB30	VDDC_BB30
AL29	VDDC_AL29	BB32	VDDC_BB32
AL31	VDDC_AL31	BB34	VDDC_BB34
AL33	VDDC_AL33	BB36	VDDC_BB36
AL35	VDDC_AL35	BB38	VDDC_BB38
AL37	VDDC_AL37	BB40	VDDC_BB40
AL39	VDDC_AL39	BC21	VDDC_BC21
AM26	VDDC_AM26	BC23	VDDC_BC23
AM28	VDDC_AM28	BC25	VDDC_BC25
AM30	VDDC_AM30	BC27	VDDC_BC27
AM32	VDDC_AM32	BC29	VDDC_BC29
AM34	VDDC_AM34	BC31	VDDC_BC31
AM36	VDDC_AM36	BC33	VDDC_BC33
AM38	VDDC_AM38	BC35	VDDC_BC35
AM40	VDDC_AM40	BC37	VDDC_BC37
AN25	VDDC_AN25	BC39	VDDC_BC39
AN27	VDDC_AN27	BD26	VDDC_BD26
AN29	VDDC_AN29	BD28	VDDC_BD28
AN31	VDDC_AN31	BD30	VDDC_BD30
AN33	VDDC_AN33	BD32	VDDC_BD32
AN35	VDDC_AN35	BD34	VDDC_BD34
AN37	VDDC_AN37	BD36	VDDC_BD36
AN39	VDDC_AN39	BD38	VDDC_BD38
AP26	VDDC_AP26	BD40	VDDC_BD40
AP28	VDDC_AP28	BE25	VDDC_BE25
AP30	VDDC_AP30	BE27	VDDC_BE27
AP32	VDDC_AP32	BE29	VDDC_BE29
AP34	VDDC_AP34	BE31	VDDC_BE31
AP36	VDDC_AP36	BE33	VDDC_BE33
AP38	VDDC_AP38	BE35	VDDC_BE35
AP40	VDDC_AP40	BE37	VDDC_BE37
AR21	VDDC_AR21	BE39	VDDC_BE39
AR23	VDDC_AR23	BF26	VDDC_BF26
AR25	VDDC_AR25	BF28	VDDC_BF28
AR27	VDDC_AR27	BF30	VDDC_BF30
AR29	VDDC_AR29	BF32	VDDC_BF32
AR31	VDDC_AR31	BF34	VDDC_BF34

BCM88690

U26L

ROV_CORE

BF36	VDDC_BF36	AK42	FAB_VDDC_AK42
BF38	VDDC_BF38	AL41	FAB_VDDC_AL41
BF40	VDDC_BF40	AM42	FAB_VDDC_AM42
BG25	VDDC_BG25	AN41	FAB_VDDC_AN41
BG27	VDDC_BG27	AR41	FAB_VDDC_AR41
BG29	VDDC_BG29	AT42	FAB_VDDC_AT42
BG31	VDDC_BG31	AU41	FAB_VDDC_AU41
BG33	VDDC_BG33	AV42	FAB_VDDC_AV42
BG35	VDDC_BG35	AW41	FAB_VDDC_AW41
BG37	VDDC_BG37	AY42	FAB_VDDC_AY42
BG39	VDDC_BG39	BA41	FAB_VDDC_BA41
BH26	VDDC_BH26	BB42	FAB_VDDC_BB42
BH28	VDDC_BH28	BC41	FAB_VDDC_BC41
BH30	VDDC_BH30	BD42	FAB_VDDC_BD42
BH32	VDDC_BH32	BE41	FAB_VDDC_BE41
BH34	VDDC_BH34	BF42	FAB_VDDC_BF42
BH36	VDDC_BH36	BG41	FAB_VDDC_BG41
BH38	VDDC_BH38	BJ41	FAB_VDDC_BJ41
BH40	VDDC_BH40	BK42	FAB_VDDC_BK42
BJ25	VDDC_BJ25	AD36	U_VDDC_AD36
BJ27	VDDC_BJ27	AE33	U_VDDC_AE33
BJ29	VDDC_BJ29	AE35	U_VDDC_AE35
BJ31	VDDC_BJ31	BK40	VDDC_BK40
BJ33	VDDC_BJ33	BL27	VDDC_BL27
BJ35	VDDC_BJ35	BL29	VDDC_BL29
BJ37	VDDC_BJ37	BL31	VDDC_BL31
BJ39	VDDC_BJ39	BL33	VDDC_BL33
BK26	VDDC_BK26	BL35	VDDC_BL35
BK28	VDDC_BK28	BL37	VDDC_BL37
BK30	VDDC_BK30	BL39	VDDC_BL39
BK32	VDDC_BK32	BL41	VDDC_BL41
BK34	VDDC_BK34	BM26	VDDC_BM26
BK36	VDDC_BK36	BM28	VDDC_BM28
BK38	VDDC_BK38	BM30	VDDC_BM30
BN41	VDDC_BN41	BM32	VDDC_BM32
BN43	VDDC_BN43	BM34	VDDC_BM34
		BM36	VDDC_BM36
		BM38	VDDC_BM38
		BM40	VDDC_BM40
		BM42	VDDC_BM42
		BM44	VDDC_BM44
		BN27	VDDC_BN27
		BN29	VDDC_BN29
		BN31	VDDC_BN31
		BN33	VDDC_BN33
		BN35	VDDC_BN35
		BN37	VDDC_BN37
		BN39	VDDC_BN39

BCM88690

[140] FAP_VDDC_SENSE_P — AW27 VDDC_SENSE
[140] FAP_VSS_SENSE_N — AV27 VSS_SENSE

FAB_VDDC_SENSE_P — M52 FAB_VDDC_SENSE
FAB_VSS_SENSE_N — M51 FAB_VSS_SENSE
TP226, TP227

NIF0_VDDC_SENSE_P — AB20 NIF0_VDDC_SENSE
NIF0_VSS_SENSE_N — AA20 NIF0_VSS_SENSE
NIF1_VDDC_SENSE_P — BR27 NIF1_VDDC_SENSE
NIF1_VSS_SENSE_N — BP27 NIF1_VSS_SENSE
TP243, TP240, TP259, TP255

U_VDDC_SENSE_P — AC36 U_VDDC_SENSE
U_VSS_SENSE_N — AB36 U_VSS_SENSE
TP244, TP242

P1V8 — L118 3A,0.03ohm 60ohm — 70mA — FAP_FAB_LCPLL0_AVDD1P8
C1060 1uF 6.3V; C1082 47uF 4V; C1080 4.7uF 6.3V; C1238 0.1uF 10V; C1251 0.1uF 10V
GND

P1V8 — L147 3A,0.03ohm 60ohm — 70mA — FAP_FAB_LCPLL1_AVDD1P8
C2533 1uF 6.3V; C2521 47uF 4V; C2516 4.7uF 6.3V; C2463 0.1uF 10V; C2467 0.1uF 10V
GND

P1V8 — L121 3A,0.03ohm 60ohm — 70mA — FAP_UPLL_AVDD1P8
C1062 1uF 6.3V; C1075 47uF 4V; C1089 4.7uF 6.3V; C1317 0.1uF 10V; C1312 0.1uF 10V
GND

P1V8 — L148 3A,0.03ohm 60ohm — 70mA — FAP_CPLL_AVDD1P8
C2559 1uF 6.3V; C2544 47uF 4V; C2543 4.7uF 6.3V; C2019 0.1uF 10V; C1977 0.1uF 10V
GND

P1V8 — L145 3A,0.03ohm 60ohm — 70mA — FAP_NIF_LCPLL1_AVDD1P8
C2538 1uF 6.3V; C2522 47uF 4V; C2518 4.7uF 6.3V; C2464 0.1uF 10V; C2465 0.1uF 10V
GND

FAP_CPLL_AVDD1P8 — AW32 C_PLL_AVDD1P8
C4360 2.0.1uF; C4364 2.0.1uF — AU33 C_PLL_AGND_AU33; AW33 C_PLL_AGND_AW33
GND

FAP_FAB_LCPLL0_AVDD1P8 — V50 FAB_LCPLL0_AVDD1P8
FAP_FAB_LCPLL1_AVDD1P8 — BR38 FAB_LCPLL1_AVDD1P8

FAP_NIF_LCPLL0_AVDD1P8 — AA17 NIF_LCPLL0_AVDD1P8
FAP_NIF_LCPLL1_AVDD1P8 — BR21 NIF_LCPLL1_AVDD1P8

FAP_PCIE_TRVDD0P8 — H33 PCIE_RTVDD0P8_H33
FAP_PCIE_PVDD0P8 — J33 PCIE_RTVDD0P8_J33; A34 PCIE_PVDD0P8

FAP_SYNCE_PLL_AVDD1P8 — W21 SYNCE_PLL_VDD1P8
GND
C4361 2.0.1uF — FAP_UPLL_AVDD1P8 — AB34 U_PLL_AGND; AA34 U_PLL_AVDD1P8

FAP_TS_PLL_AVDD1P8 — Y34 TS_PLL_VDD1P8

P3V3 — P3V3

U26M

N50	VDDO_3P3_N50
R19	VDDO_3P3_R19
R21	VDDO_3P3_R21
R23	VDDO_3P3_R23
V19	VDDO_3P3_V19
A11	VDDO_3P3_A11
A23	VDDO_3P3_A23
A27	VDDO_3P3_A27
A5	VDDO_3P3_A5
A8	VDDO_3P3_A8
B3	VDDO_3P3_B3
D26	VDDO_3P3_D26
E6	VDDO_3P3_E6
E10	VDDO_3P3_E10
E24	VDDO_3P3_E24
F27	VDDO_3P3_F27
G13	VDDO_3P3_G13
G15	VDDO_3P3_G15
G19	VDDO_3P3_G19
G21	VDDO_3P3_G21
G24	VDDO_3P3_G24
G37	VDDO_3P3_G37
G40	VDDO_3P3_G40
H10	VDDO_3P3_H10
J6	VDDO_3P3_J6
J27	VDDO_3P3_J27
K16	VDDO_3P3_K16
K18	VDDO_3P3_K18
K24	VDDO_3P3_K24
K35	VDDO_3P3_K35
K38	VDDO_3P3_K38
L20	VDDO_3P3_L20
L22	VDDO_3P3_L22
L31	VDDO_3P3_L31
L40	VDDO_3P3_L40
M44	VDDO_3P3_M44
N15	VDDO_3P3_N15
N17	VDDO_3P3_N17

BCM88690

P3V3

C1103 1uF 6.3V; C1099 1uF 6.3V; C1128 1uF 6.3V; C1113 1uF 6.3V; C1100 1uF 6.3V; C1114 1uF 6.3V; C1139 1uF 6.3V; C1138 1uF 6.3V; C1140 1uF 6.3V; C1115 1uF 6.3V; C1101 10nF; C1190 10nF; C1127 10nF; C1118 10nF; C1141 10nF; C1095 10nF; C1170 10nF; C1122 10nF; C1153 10nF
C1112 0.1uF 10V; C1134 0.1uF 10V; C1142 0.1uF 10V; C1126 0.1uF 10V; C1123 0.1uF 10V; C1098 0.1uF 10V; C1132 0.1uF 10V; C1116 0.1uF 10V; C1143 0.1uF 10V; C1250 0.1uF 10V; C1169 0.1uF 10V; C1196 0.1uF 10V; C1137 0.1uF 10V; C1136 0.1uF 10V; C1188 0.1uF 10V; C1120 0.1uF 10V; C1125 0.1uF 10V; C1131 0.1uF 10V
GND

P1V8 — L123 3A,0.03ohm 60ohm — 20mA — FAP_SYNCE_PLL_AVDD1P8
C1064 1uF 6.3V; C1077 47uF 4V; C1092 4.7uF 6.3V; C1266 0.1uF 10V
GND

P1V8 — L120 3A,0.03ohm 60ohm — 20mA — FAP_TS_PLL_AVDD1P8
C1063 1uF 6.3V; C1073 47uF 4V; C1088 4.7uF 6.3V; C1304 0.1uF 10V
GND

0V8_MAC — L126 3A,0.03ohm 60ohm — 25mA — FAP_PCIE_TRVDD0P8
C1084 1uF 6.3V; C1129 10uF 6.3V; C1121 0.1uF 10V; C1130 0.1uF 10V; C1133 0.1uF 10V; C1124 0.1uF 10V
GND

0V8_MAC — L125 3A,0.03ohm 60ohm — 150mA — FAP_PCIE_PVDD0P8
C1081 1uF 6.3V; C1094 10uF 6.3V; C1096 0.1uF 10V
GND

P1V8 — L396 3A,0.03ohm 60ohm — 70mA — FAP_NIF_LCPLL0_AVDD1P8
C3699 1uF 6.3V; C3700 47uF 4V; C3701 4.7uF 6.3V; C3702 0.1uF 10V; C3703 0.1uF 10V
GND

<Core Design>

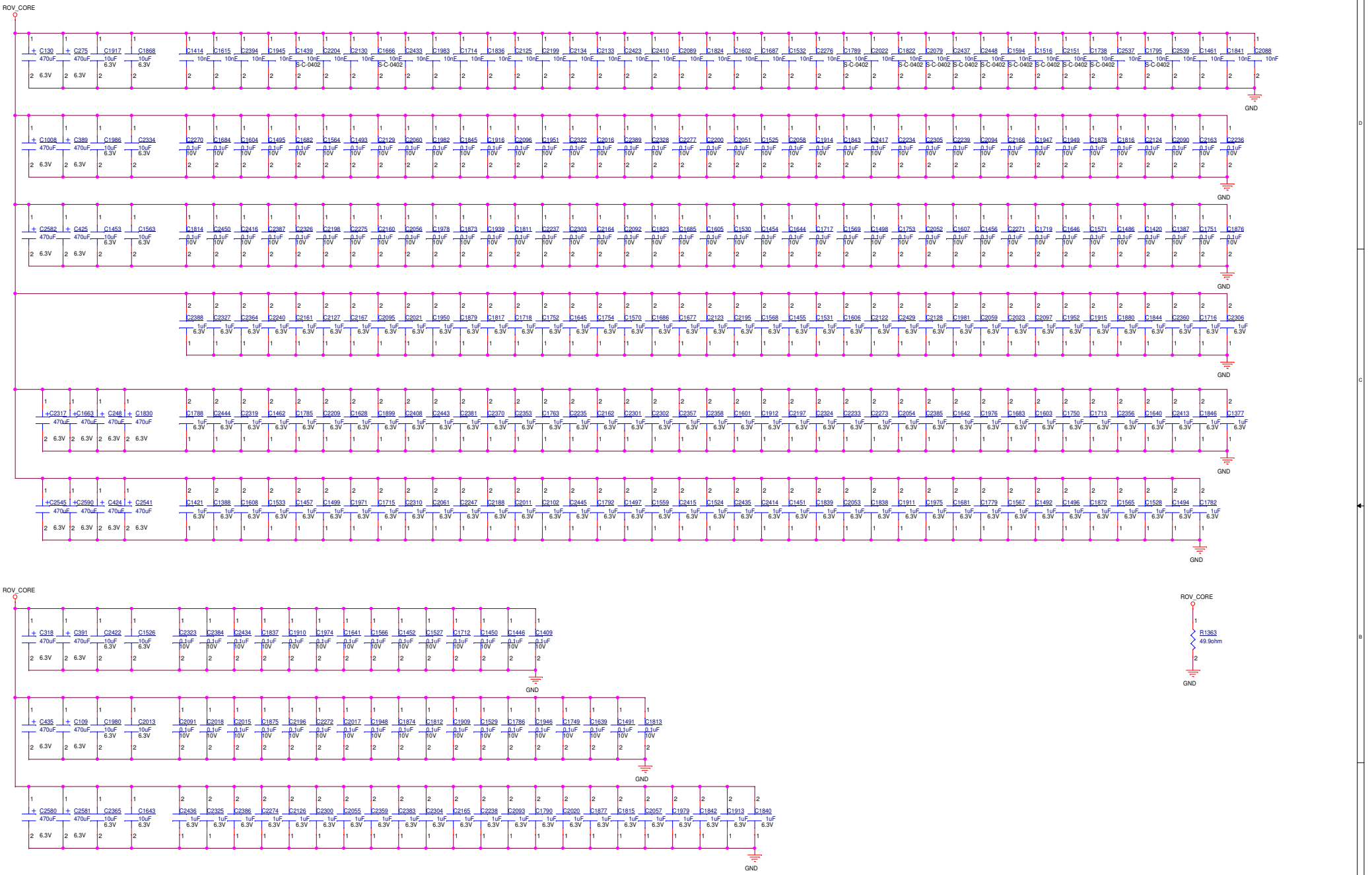
UfiSpace Co., Ltd.

Title: 009_Jericho2_VDDC_VDDO_PCIE_PLL

Document Number: PCB P/N: T99O114T00

Sheet 9 of 152

Rev 015

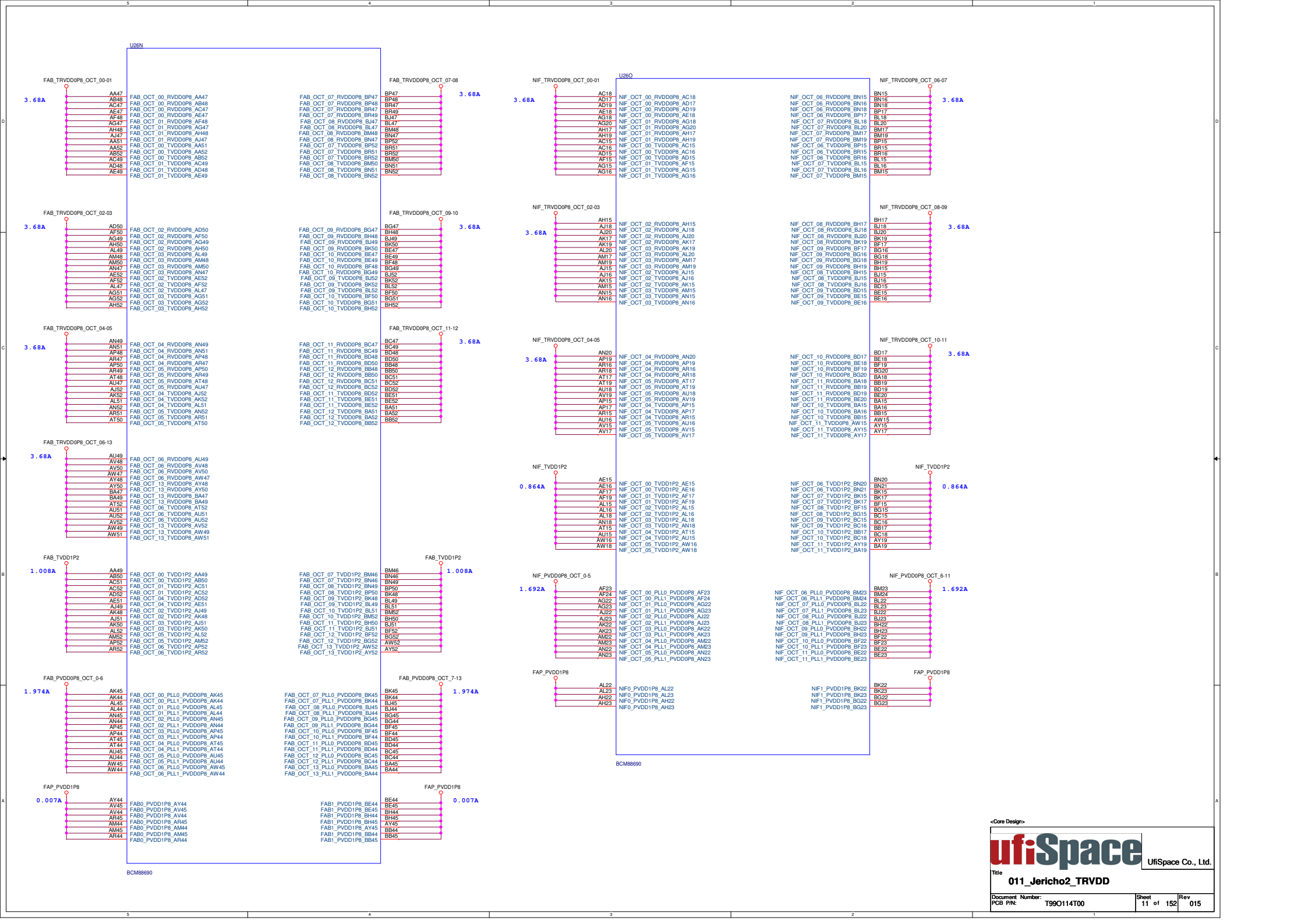


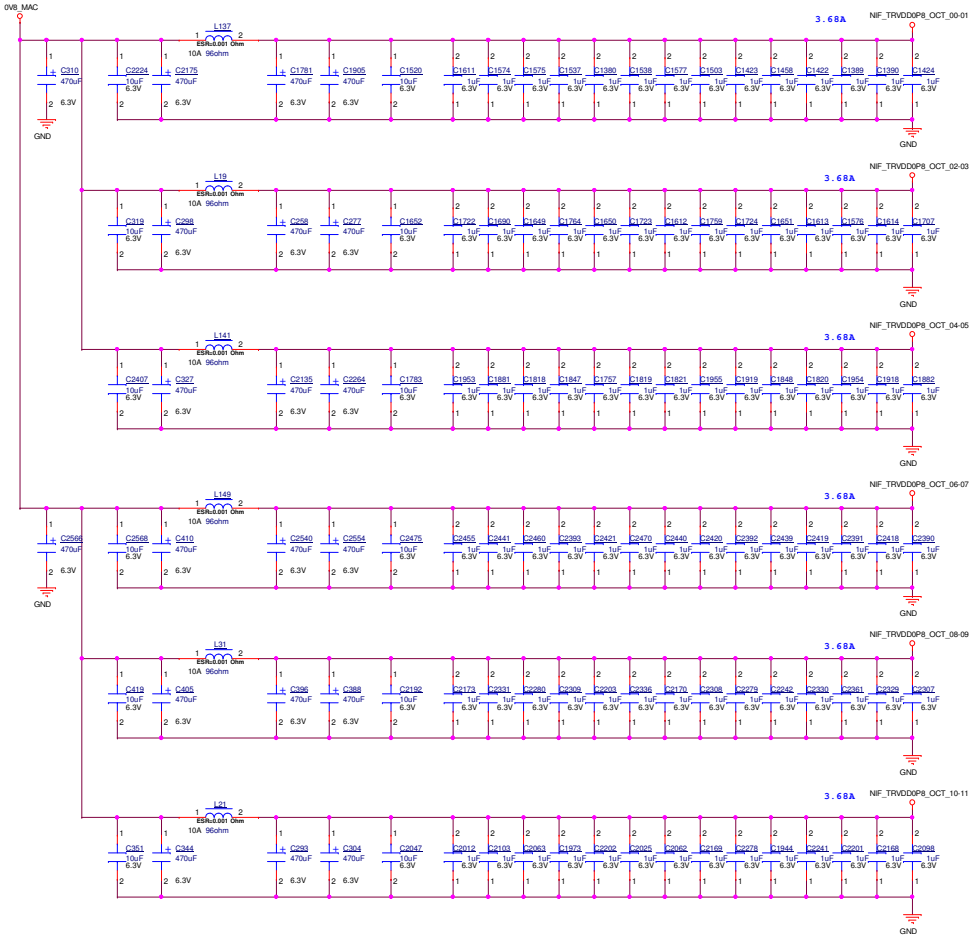
<Core Design>

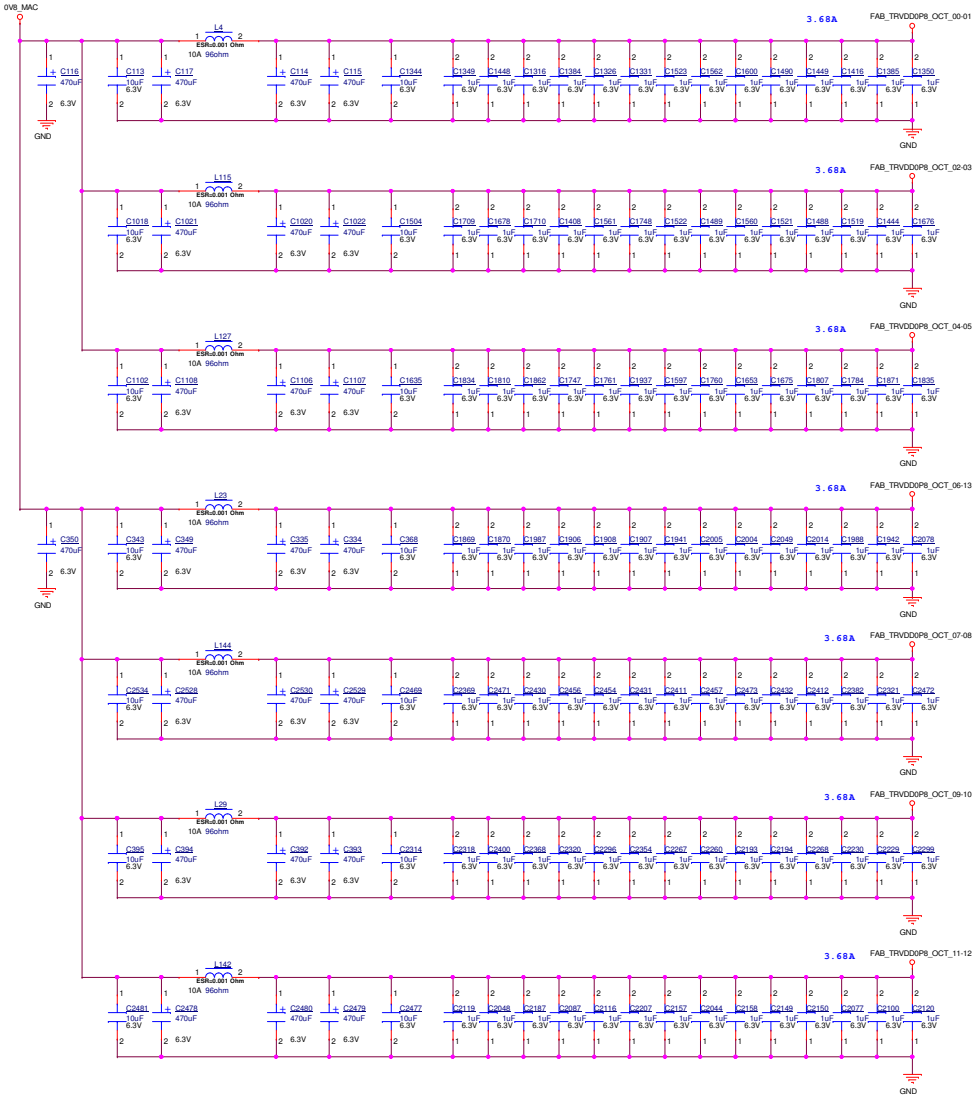
ufiSpace UfiSpace Co., Ltd.

Title: 010_Jericho2_VDDC_Caps

Document Number: PCB P/N: T99O114T00	Sheet 10 of 152	Rev 015


U26N
FAB_TRVDD0P8_OCT_00-01
3.68A
AA47 AB48 AC47 AE47 AF48 AG47 AH48 AJ47 AA51 AA52 AB52 AC49 AD48 AE49
FAB_OCT_00_RVDD0P8_AA47 FAB_OCT_00_RVDD0P8_AB48 FAB_OCT_00_RVDD0P8_AC47 FAB_OCT_00_RVDD0P8_AE47 FAB_OCT_01_RVDD0P8_AF48 FAB_OCT_01_RVDD0P8_AG47 FAB_OCT_01_RVDD0P8_AH48 FAB_OCT_01_RVDD0P8_AJ47 FAB_OCT_00_TVDD0P8_AA51 FAB_OCT_00_TVDD0P8_AA52 FAB_OCT_00_TVDD0P8_AB52 FAB_OCT_01_TVDD0P8_AC49 FAB_OCT_01_TVDD0P8_AD48 FAB_OCT_01_TVDD0P8_AE49
FAB_TRVDD0P8_OCT_07-08
3.68A
BP47 BP48 BP47 BP47 BP49 BJ47 BL47 BM48 BN47 BP52 BR51 BR52 BR50 BN51 BN52
FAB_OCT_07_RVDD0P8_BP47 FAB_OCT_07_RVDD0P8_BP48 FAB_OCT_07_RVDD0P8_BR47 FAB_OCT_07_RVDD0P8_BR49 FAB_OCT_08_RVDD0P8_BJ47 FAB_OCT_08_RVDD0P8_BL47 FAB_OCT_08_RVDD0P8_BM48 FAB_OCT_08_RVDD0P8_BN47 FAB_OCT_07_TVDD0P8_BP52 FAB_OCT_07_TVDD0P8_BR51 FAB_OCT_07_TVDD0P8_BR52 FAB_OCT_08_TVDD0P8_BM50 FAB_OCT_08_TVDD0P8_BN51 FAB_OCT_08_TVDD0P8_BN52
FAB_TRVDD0P8_OCT_02-03
3.68A
AD50 AF50 AG49 AH50 AL49 AM48 AM50 AN47 AE52 AF52 AL47 AG51 AG52 AH52
FAB_OCT_02_RVDD0P8_AD50 FAB_OCT_02_RVDD0P8_AF50 FAB_OCT_02_RVDD0P8_AG49 FAB_OCT_02_RVDD0P8_AH50 FAB_OCT_03_RVDD0P8_AL49 FAB_OCT_03_RVDD0P8_AM48 FAB_OCT_03_RVDD0P8_AM50 FAB_OCT_03_RVDD0P8_AN47 FAB_OCT_02_TVDD0P8_AE52 FAB_OCT_02_TVDD0P8_AF52 FAB_OCT_02_TVDD0P8_AL47 FAB_OCT_03_TVDD0P8_AG51 FAB_OCT_03_TVDD0P8_AG52 FAB_OCT_03_TVDD0P8_AH52
FAB_TRVDD0P8_OCT_09-10
3.68A
BG47 BH48 BJ49 BK50 BE47 BE49 BF48 BG49 BJ52 BK52 BL52 BF50 BG51 BH52
FAB_OCT_09_RVDD0P8_BG47 FAB_OCT_09_RVDD0P8_BH48 FAB_OCT_09_RVDD0P8_BJ49 FAB_OCT_09_RVDD0P8_BK50 FAB_OCT_10_RVDD0P8_BE47 FAB_OCT_10_RVDD0P8_BE49 FAB_OCT_10_RVDD0P8_BF48 FAB_OCT_10_RVDD0P8_BG49 FAB_OCT_09_TVDD0P8_BJ52 FAB_OCT_09_TVDD0P8_BK52 FAB_OCT_09_TVDD0P8_BL52 FAB_OCT_10_TVDD0P8_BF50 FAB_OCT_10_TVDD0P8_BG51 FAB_OCT_10_TVDD0P8_BH52
FAB_TRVDD0P8_OCT_04-05
3.68A
AN49 AN51 AP48 AR47 AP50 AR49 AT48 AU47 AJ52 AK52 AL51 AN52 AR51 AT50
FAB_OCT_04_RVDD0P8_AN49 FAB_OCT_04_RVDD0P8_AN51 FAB_OCT_04_RVDD0P8_AP48 FAB_OCT_04_RVDD0P8_AR47 FAB_OCT_05_RVDD0P8_AP50 FAB_OCT_05_RVDD0P8_AR49 FAB_OCT_05_RVDD0P8_AT48 FAB_OCT_05_RVDD0P8_AU47 FAB_OCT_04_TVDD0P8_AJ52 FAB_OCT_04_TVDD0P8_AK52 FAB_OCT_04_TVDD0P8_AL51 FAB_OCT_05_TVDD0P8_AN52 FAB_OCT_05_TVDD0P8_AR51 FAB_OCT_05_TVDD0P8_AT50
FAB_TRVDD0P8_OCT_11-12
3.68A
BC47 BC49 BD48 BD50 BB48 BB50 BC51 BC52 BD52 BE51 BE52 BA51 BA52 BB52
FAB_OCT_11_RVDD0P8_BC47 FAB_OCT_11_RVDD0P8_BC49 FAB_OCT_11_RVDD0P8_BD48 FAB_OCT_11_RVDD0P8_BD50 FAB_OCT_12_RVDD0P8_BB48 FAB_OCT_12_RVDD0P8_BB50 FAB_OCT_12_RVDD0P8_BC51 FAB_OCT_12_RVDD0P8_BC52 FAB_OCT_11_TVDD0P8_BD52 FAB_OCT_11_TVDD0P8_BE51 FAB_OCT_11_TVDD0P8_BE52 FAB_OCT_12_TVDD0P8_BA51 FAB_OCT_12_TVDD0P8_BA52 FAB_OCT_12_TVDD0P8_BB52
FAB_TRVDD0P8_OCT_06-13
3.68A
AU49 AV48 AV50 AW47 AY48 AY50 BA47 BA49 AT52 AU51 AU52 AV52 AW49 AW51
FAB_OCT_06_RVDD0P8_AU49 FAB_OCT_06_RVDD0P8_AV48 FAB_OCT_06_RVDD0P8_AV50 FAB_OCT_06_RVDD0P8_AW47 FAB_OCT_13_RVDD0P8_AY48 FAB_OCT_13_RVDD0P8_AY50 FAB_OCT_13_RVDD0P8_BA47 FAB_OCT_13_RVDD0P8_BA49 FAB_OCT_06_TVDD0P8_AT52 FAB_OCT_06_TVDD0P8_AU51 FAB_OCT_06_TVDD0P8_AU52 FAB_OCT_13_TVDD0P8_AV52 FAB_OCT_13_TVDD0P8_AW49 FAB_OCT_13_TVDD0P8_AW51
FAB_TVDD1P2
1.008A
AA49 AB50 AC51 AC52 AD52 AE51 AJ49 AK48 AJ51 AK50 AL52 AM52 AP52 AR52
FAB_OCT_00_TVDD1P2_AA49 FAB_OCT_00_TVDD1P2_AB50 FAB_OCT_01_TVDD1P2_AC51 FAB_OCT_01_TVDD1P2_AC52 FAB_OCT_04_TVDD1P2_AD52 FAB_OCT_04_TVDD1P2_AE51 FAB_OCT_02_TVDD1P2_AJ49 FAB_OCT_02_TVDD1P2_AK48 FAB_OCT_03_TVDD1P2_AJ51 FAB_OCT_03_TVDD1P2_AK50 FAB_OCT_05_TVDD1P2_AL52 FAB_OCT_05_TVDD1P2_AM52 FAB_OCT_06_TVDD1P2_AP52 FAB_OCT_06_TVDD1P2_AR52
FAB_TVDD1P2
1.008A
BM46 BN46 BN49 BP50 BK48 BL49 BL51 BM52 BH50 BJ51 BF52 BG52 AW52 AY52
FAB_OCT_07_TVDD1P2_BM46 FAB_OCT_07_TVDD1P2_BN46 FAB_OCT_08_TVDD1P2_BN49 FAB_OCT_08_TVDD1P2_BP50 FAB_OCT_09_TVDD1P2_BK48 FAB_OCT_09_TVDD1P2_BL49 FAB_OCT_10_TVDD1P2_BL51 FAB_OCT_10_TVDD1P2_BM52 FAB_OCT_11_TVDD1P2_BH50 FAB_OCT_11_TVDD1P2_BJ51 FAB_OCT_12_TVDD1P2_BF52 FAB_OCT_12_TVDD1P2_BG52 FAB_OCT_13_TVDD1P2_AW52 FAB_OCT_13_TVDD1P2_AY52
FAB_PVDD0P8_OCT_0-6
1.974A
AK45 AK44 AL45 AL44 AN45 AN44 AP45 AP44 AT45 AT44 AU45 AU44 AW45 AW44
FAB_OCT_00_PLL0_PVDD0P8_AK45 FAB_OCT_00_PLL1_PVDD0P8_AK44 FAB_OCT_01_PLL0_PVDD0P8_AL45 FAB_OCT_01_PLL1_PVDD0P8_AL44 FAB_OCT_02_PLL0_PVDD0P8_AN45 FAB_OCT_02_PLL1_PVDD0P8_AN44 FAB_OCT_03_PLL0_PVDD0P8_AP45 FAB_OCT_03_PLL1_PVDD0P8_AP44 FAB_OCT_04_PLL0_PVDD0P8_AT45 FAB_OCT_04_PLL1_PVDD0P8_AT44 FAB_OCT_05_PLL0_PVDD0P8_AU45 FAB_OCT_05_PLL1_PVDD0P8_AU44 FAB_OCT_06_PLL0_PVDD0P8_AW45 FAB_OCT_06_PLL1_PVDD0P8_AW44
FAB_PVDD0P8_OCT_7-13
1.974A
BK45 BK44 BJ45 BJ44 BG45 BG44 BF45 BF44 BD45 BD44 BC45 BC44 BA45 BA44
FAB_OCT_07_PLL0_PVDD0P8_BK45 FAB_OCT_07_PLL1_PVDD0P8_BK44 FAB_OCT_08_PLL0_PVDD0P8_BJ45 FAB_OCT_08_PLL1_PVDD0P8_BJ44 FAB_OCT_09_PLL0_PVDD0P8_BG45 FAB_OCT_09_PLL1_PVDD0P8_BG44 FAB_OCT_10_PLL0_PVDD0P8_BF45 FAB_OCT_10_PLL1_PVDD0P8_BF44 FAB_OCT_11_PLL0_PVDD0P8_BD45 FAB_OCT_11_PLL1_PVDD0P8_BD44 FAB_OCT_12_PLL0_PVDD0P8_BC45 FAB_OCT_12_PLL1_PVDD0P8_BC44 FAB_OCT_13_PLL0_PVDD0P8_BA45 FAB_OCT_13_PLL1_PVDD0P8_BA44
FAP_PVDD1P8
0.007A
AY44 AV45 AV44 AR45 AM44 AM45 AR44
FAB0_PVDD1P8_AY44 FAB0_PVDD1P8_AV45 FAB0_PVDD1P8_AV44 FAB0_PVDD1P8_AR45 FAB0_PVDD1P8_AM44 FAB0_PVDD1P8_AM45 FAB0_PVDD1P8_AR44
FAP_PVDD1P8
0.007A
BE44 BE45 BH44 BH45 AY45 BB44 BB45
FAB1_PVDD1P8_BE44 FAB1_PVDD1P8_BE45 FAB1_PVDD1P8_BH44 FAB1_PVDD1P8_BH45 FAB1_PVDD1P8_AY45 FAB1_PVDD1P8_BB44 FAB1_PVDD1P8_BB45
BCM88690
U26O
NIF_TRVDD0P8_OCT_00-01
3.68A
AC18 AD17 AD19 AE18 AG18 AG20 AH17 AH19 AC15 AC16 AD15 AF15 AG15 AG16
NIF_OCT_00_RVDD0P8_AC18 NIF_OCT_00_RVDD0P8_AD17 NIF_OCT_00_RVDD0P8_AD19 NIF_OCT_00_RVDD0P8_AE18 NIF_OCT_01_RVDD0P8_AG18 NIF_OCT_01_RVDD0P8_AG20 NIF_OCT_01_RVDD0P8_AH17 NIF_OCT_01_RVDD0P8_AH19 NIF_OCT_00_TVDD0P8_AC15 NIF_OCT_00_TVDD0P8_AC16 NIF_OCT_00_TVDD0P8_AD15 NIF_OCT_01_TVDD0P8_AF15 NIF_OCT_01_TVDD0P8_AG15 NIF_OCT_01_TVDD0P8_AG16
NIF_TRVDD0P8_OCT_06-07
3.68A
BN15 BN16 BN18 BP17 BL18 BL20 BM17 BM19 BP15 BR15 BR16 BL15 BL16 BM15
NIF_OCT_06_RVDD0P8_BN15 NIF_OCT_06_RVDD0P8_BN16 NIF_OCT_06_RVDD0P8_BN18 NIF_OCT_06_RVDD0P8_BP17 NIF_OCT_07_RVDD0P8_BL18 NIF_OCT_07_RVDD0P8_BL20 NIF_OCT_07_RVDD0P8_BM17 NIF_OCT_07_RVDD0P8_BM19 NIF_OCT_06_TVDD0P8_BP15 NIF_OCT_06_TVDD0P8_BR15 NIF_OCT_06_TVDD0P8_BR16 NIF_OCT_07_TVDD0P8_BL15 NIF_OCT_07_TVDD0P8_BL16 NIF_OCT_07_TVDD0P8_BM15
NIF_TRVDD0P8_OCT_02-03
3.68A
AH15 AJ18 AJ20 AK17 AK19 AL20 AM17 AM19 AJ15 AJ16 AK15 AM15 AN15 AN16
NIF_OCT_02_RVDD0P8_AH15 NIF_OCT_02_RVDD0P8_AJ18 NIF_OCT_02_RVDD0P8_AJ20 NIF_OCT_02_RVDD0P8_AK17 NIF_OCT_03_RVDD0P8_AK19 NIF_OCT_03_RVDD0P8_AL20 NIF_OCT_03_RVDD0P8_AM17 NIF_OCT_03_RVDD0P8_AM19 NIF_OCT_02_TVDD0P8_AJ15 NIF_OCT_02_TVDD0P8_AJ16 NIF_OCT_02_TVDD0P8_AK15 NIF_OCT_03_TVDD0P8_AM15 NIF_OCT_03_TVDD0P8_AN15 NIF_OCT_03_TVDD0P8_AN16
NIF_TRVDD0P8_OCT_08-09
3.68A
BH17 BJ18 BJ20 BK19 BF17 BG16 BG18 BH19 BH15 BJ15 BJ16 BD15 BE15 BE16
NIF_OCT_08_RVDD0P8_BH17 NIF_OCT_08_RVDD0P8_BJ18 NIF_OCT_08_RVDD0P8_BJ20 NIF_OCT_08_RVDD0P8_BK19 NIF_OCT_09_RVDD0P8_BF17 NIF_OCT_09_RVDD0P8_BG16 NIF_OCT_09_RVDD0P8_BG18 NIF_OCT_09_RVDD0P8_BH19 NIF_OCT_08_TVDD0P8_BH15 NIF_OCT_08_TVDD0P8_BJ15 NIF_OCT_08_TVDD0P8_BJ16 NIF_OCT_09_TVDD0P8_BD15 NIF_OCT_09_TVDD0P8_BE15 NIF_OCT_09_TVDD0P8_BE16
NIF_TRVDD0P8_OCT_04-05
3.68A
AN20 AP19 AR16 AR18 AT17 AT19 AU18 AV19 AP15 AP17 AR15 AU16 AV15 AV17
NIF_OCT_04_RVDD0P8_AN20 NIF_OCT_04_RVDD0P8_AP19 NIF_OCT_04_RVDD0P8_AR16 NIF_OCT_04_RVDD0P8_AR18 NIF_OCT_05_RVDD0P8_AT17 NIF_OCT_05_RVDD0P8_AT19 NIF_OCT_05_RVDD0P8_AU18 NIF_OCT_05_RVDD0P8_AV19 NIF_OCT_04_TVDD0P8_AP15 NIF_OCT_04_TVDD0P8_AP17 NIF_OCT_04_TVDD0P8_AR15 NIF_OCT_05_TVDD0P8_AU16 NIF_OCT_05_TVDD0P8_AV15 NIF_OCT_05_TVDD0P8_AV17
NIF_TRVDD0P8_OCT_10-11
3.68A
BD17 BE18 BF19 BG20 BA18 BB19 BD19 BE20 BA15 BA16 BB15 AW15 AY15 AY17
NIF_OCT_10_RVDD0P8_BD17 NIF_OCT_10_RVDD0P8_BE18 NIF_OCT_10_RVDD0P8_BF19 NIF_OCT_10_RVDD0P8_BG20 NIF_OCT_11_RVDD0P8_BA18 NIF_OCT_11_RVDD0P8_BB19 NIF_OCT_11_RVDD0P8_BD19 NIF_OCT_11_RVDD0P8_BE20 NIF_OCT_10_TVDD0P8_BA15 NIF_OCT_10_TVDD0P8_BA16 NIF_OCT_10_TVDD0P8_BB15 NIF_OCT_11_TVDD0P8_AW15 NIF_OCT_11_TVDD0P8_AY15 NIF_OCT_11_TVDD0P8_AY17
NIF_TVDD1P2
0.864A
AE15 AE16 AF17 AF19 AL15 AL16 AL18 AN18 AT15 AU15 AW16 AW18
NIF_OCT_00_TVDD1P2_AE15 NIF_OCT_00_TVDD1P2_AE16 NIF_OCT_01_TVDD1P2_AF17 NIF_OCT_01_TVDD1P2_AF19 NIF_OCT_02_TVDD1P2_AL15 NIF_OCT_02_TVDD1P2_AL16 NIF_OCT_02_TVDD1P2_AL18 NIF_OCT_03_TVDD1P2_AL18 NIF_OCT_03_TVDD1P2_AN18 NIF_OCT_04_TVDD1P2_AT15 NIF_OCT_04_TVDD1P2_AU15 NIF_OCT_05_TVDD1P2_AW16 NIF_OCT_05_TVDD1P2_AW18
NIF_TVDD1P2
0.864A
BN20 BN21 BK15 BK17 BF15 BG15 BC15 BC16 BB17 BC18 AY19 BA19
NIF_OCT_06_TVDD1P2_BN20 NIF_OCT_06_TVDD1P2_BN21 NIF_OCT_07_TVDD1P2_BK15 NIF_OCT_07_TVDD1P2_BK17 NIF_OCT_08_TVDD1P2_BF15 NIF_OCT_08_TVDD1P2_BG15 NIF_OCT_09_TVDD1P2_BC15 NIF_OCT_09_TVDD1P2_BC16 NIF_OCT_10_TVDD1P2_BB17 NIF_OCT_10_TVDD1P2_BC18 NIF_OCT_11_TVDD1P2_AY19 NIF_OCT_11_TVDD1P2_BA19
NIF_PVDD0P8_OCT_0-5
1.692A
AF23 AF24 AG22 AG23 AJ22 AJ23 AK22 AK23 AM22 AM23 AN22 AN23
NIF_OCT_00_PLL0_PVDD0P8_AF23 NIF_OCT_00_PLL1_PVDD0P8_AF24 NIF_OCT_01_PLL0_PVDD0P8_AG22 NIF_OCT_01_PLL1_PVDD0P8_AG23 NIF_OCT_02_PLL0_PVDD0P8_AJ22 NIF_OCT_02_PLL1_PVDD0P8_AJ23 NIF_OCT_03_PLL0_PVDD0P8_AK22 NIF_OCT_03_PLL1_PVDD0P8_AK23 NIF_OCT_04_PLL0_PVDD0P8_AM22 NIF_OCT_04_PLL1_PVDD0P8_AM23 NIF_OCT_05_PLL0_PVDD0P8_AN22 NIF_OCT_05_PLL1_PVDD0P8_AN23
NIF_PVDD0P8_OCT_6-11
1.692A
BM23 BM24 BL22 BL23 BJ22 BJ23 BH22 BH23 BF22 BF23 BE22 BE23
NIF_OCT_06_PLL0_PVDD0P8_BM23 NIF_OCT_06_PLL1_PVDD0P8_BM24 NIF_OCT_07_PLL0_PVDD0P8_BL22 NIF_OCT_07_PLL1_PVDD0P8_BL23 NIF_OCT_08_PLL0_PVDD0P8_BJ22 NIF_OCT_08_PLL1_PVDD0P8_BJ23 NIF_OCT_09_PLL0_PVDD0P8_BH22 NIF_OCT_09_PLL1_PVDD0P8_BH23 NIF_OCT_10_PLL0_PVDD0P8_BF22 NIF_OCT_10_PLL1_PVDD0P8_BF23 NIF_OCT_11_PLL0_PVDD0P8_BE22 NIF_OCT_11_PLL1_PVDD0P8_BE23
FAP_PVDD1P8
AL22 AL23 AH22 AH23
NIF0_PVDD1P8_AL22 NIF0_PVDD1P8_AL23 NIF0_PVDD1P8_AH22 NIF0_PVDD1P8_AH23
FAP_PVDD1P8
BK22 BK23 BG22 BG23
NIF1_PVDD1P8_BK22 NIF1_PVDD1P8_BK23 NIF1_PVDD1P8_BG22 NIF1_PVDD1P8_BG23
BCM88690
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
011_Jericho2_TRVDD
Document Number:
PCB P/N: T99O114T00
Sheet 11 of 152
Rev 015





<Core Design>

UfiSpace Co., Ltd.

Title: 012_Jericho2_TRVDD_Caps

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	12 of 152	015

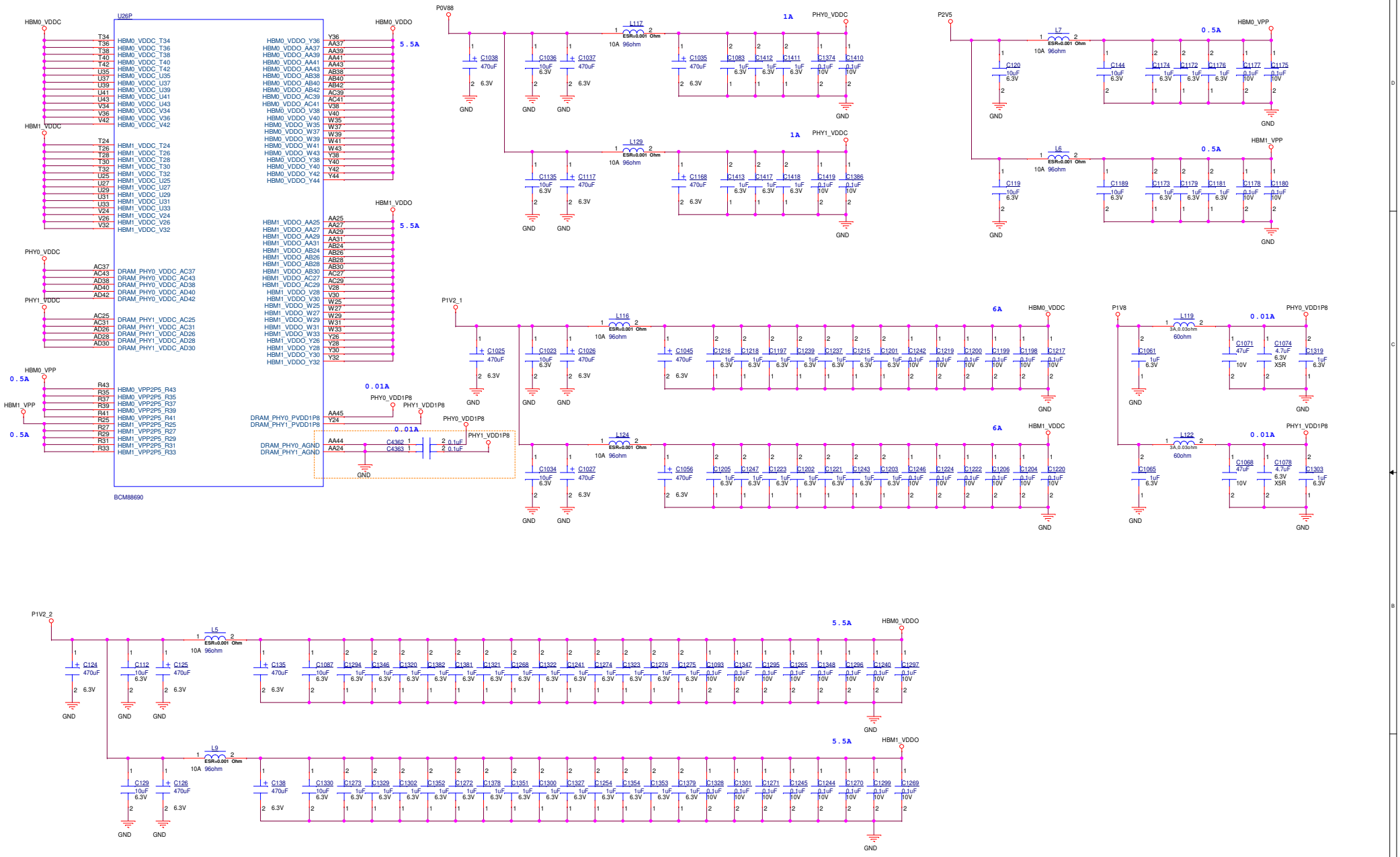


<Core Design>

UfiSpace Co., Ltd.

Title: 013_Jericho2_PVDD_TVDD1P2V_Caps

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	13 of 152	015



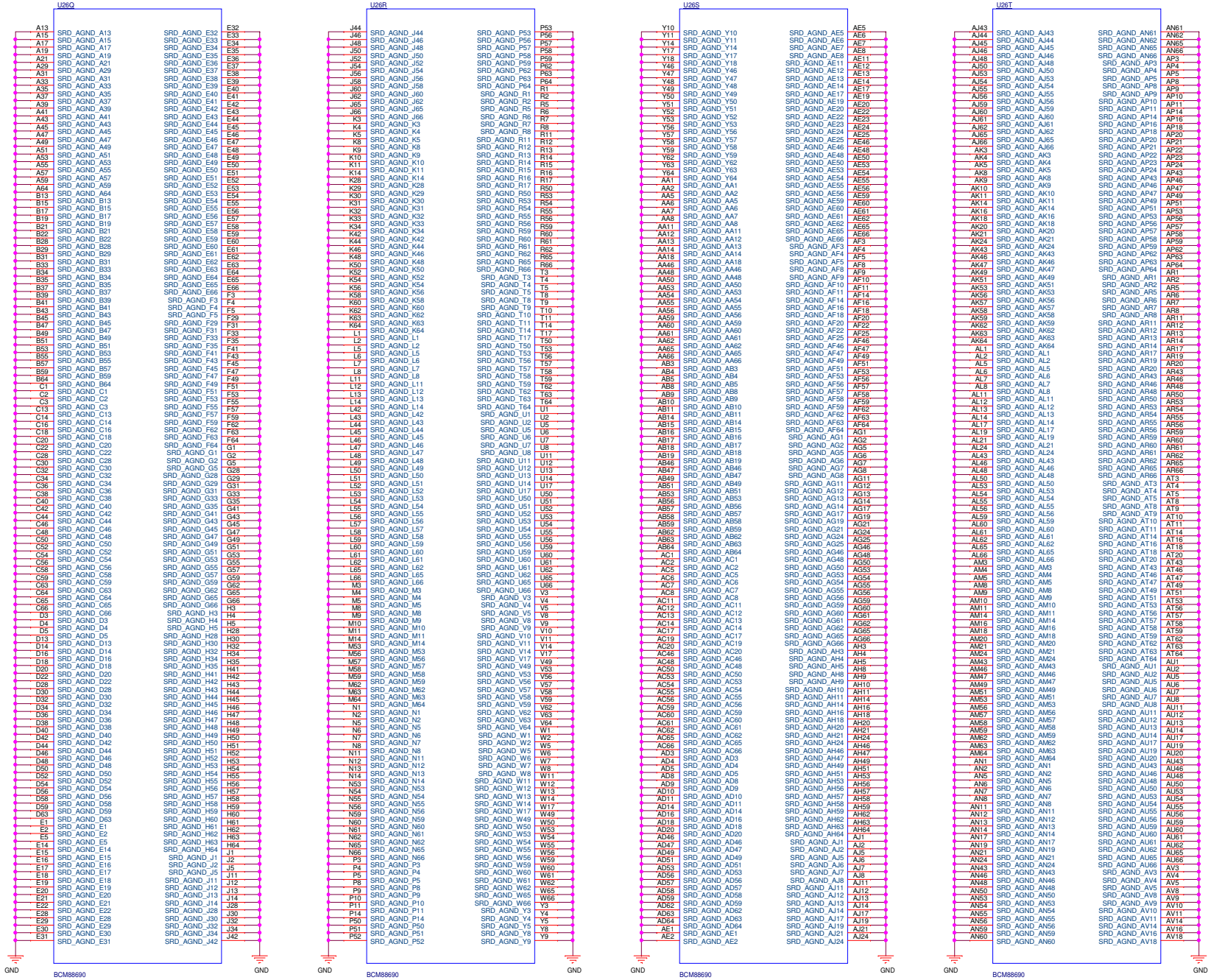
<Core Design>

UfiSpace Co., Ltd.

Title

014_Jericho2_DRAM_Power

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	14 of 152	015



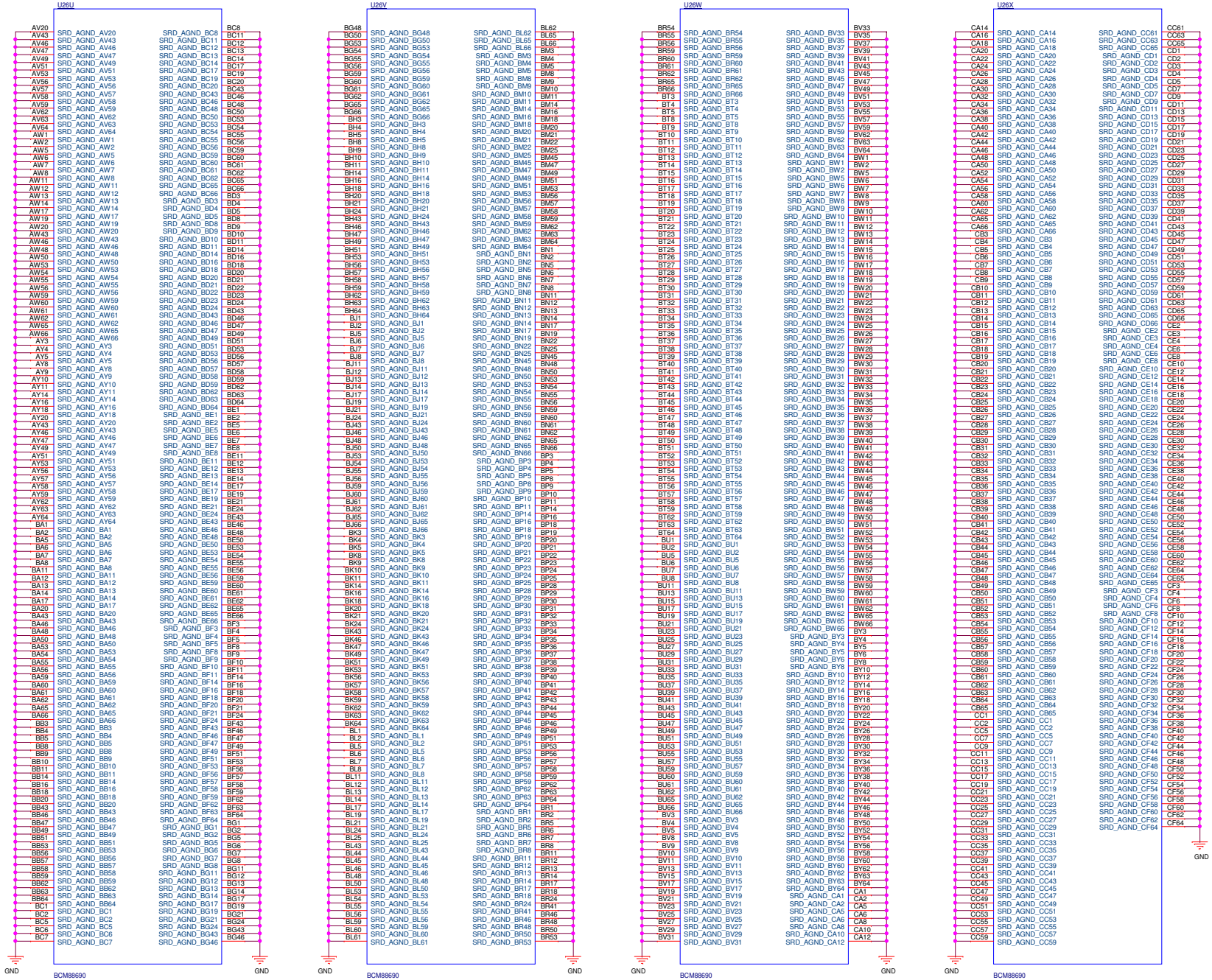
<Core Design>

UfiSpace Co., Ltd.

Title

015_Jericho2_GND1

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	15 of 152	015

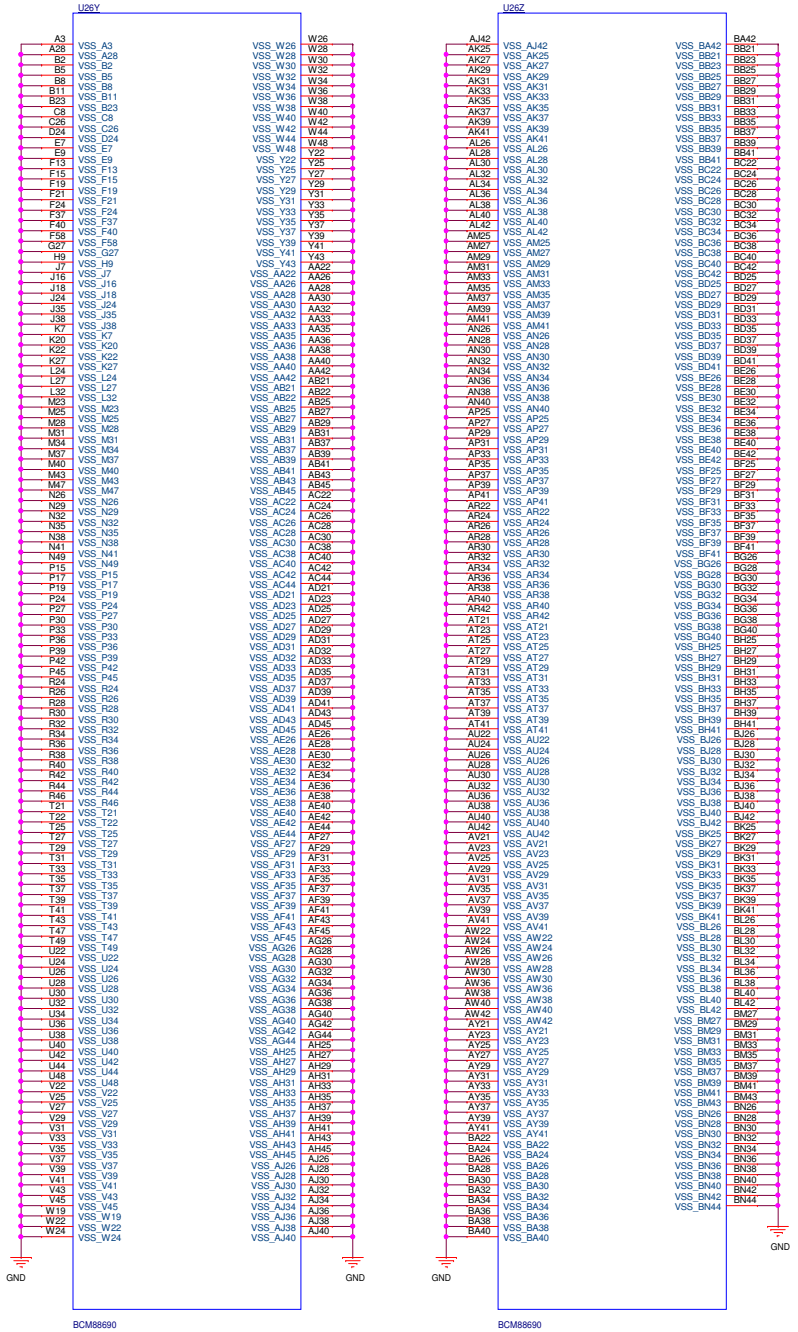


<Core Design>

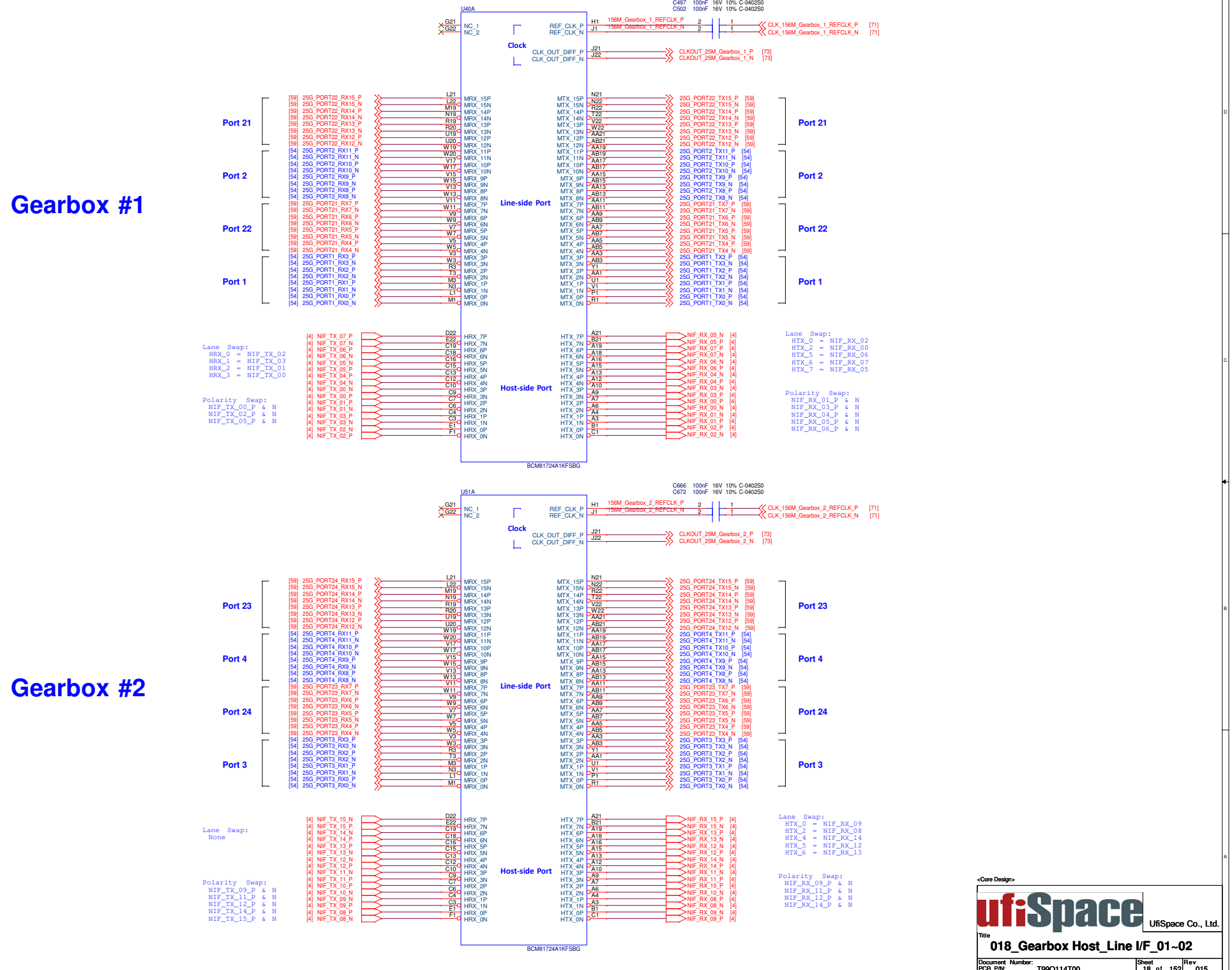
UfiSpace Co., Ltd.

Title: 016_Jericho2_GND2

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	16 of 152	015


U26Y
BCM88690
GND
U26Z
BCM88690
GND

<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
017_Jericho2_GND3
Document Number:
PCB P/N: T99O114T00
Sheet 17 of 152
Rev 015



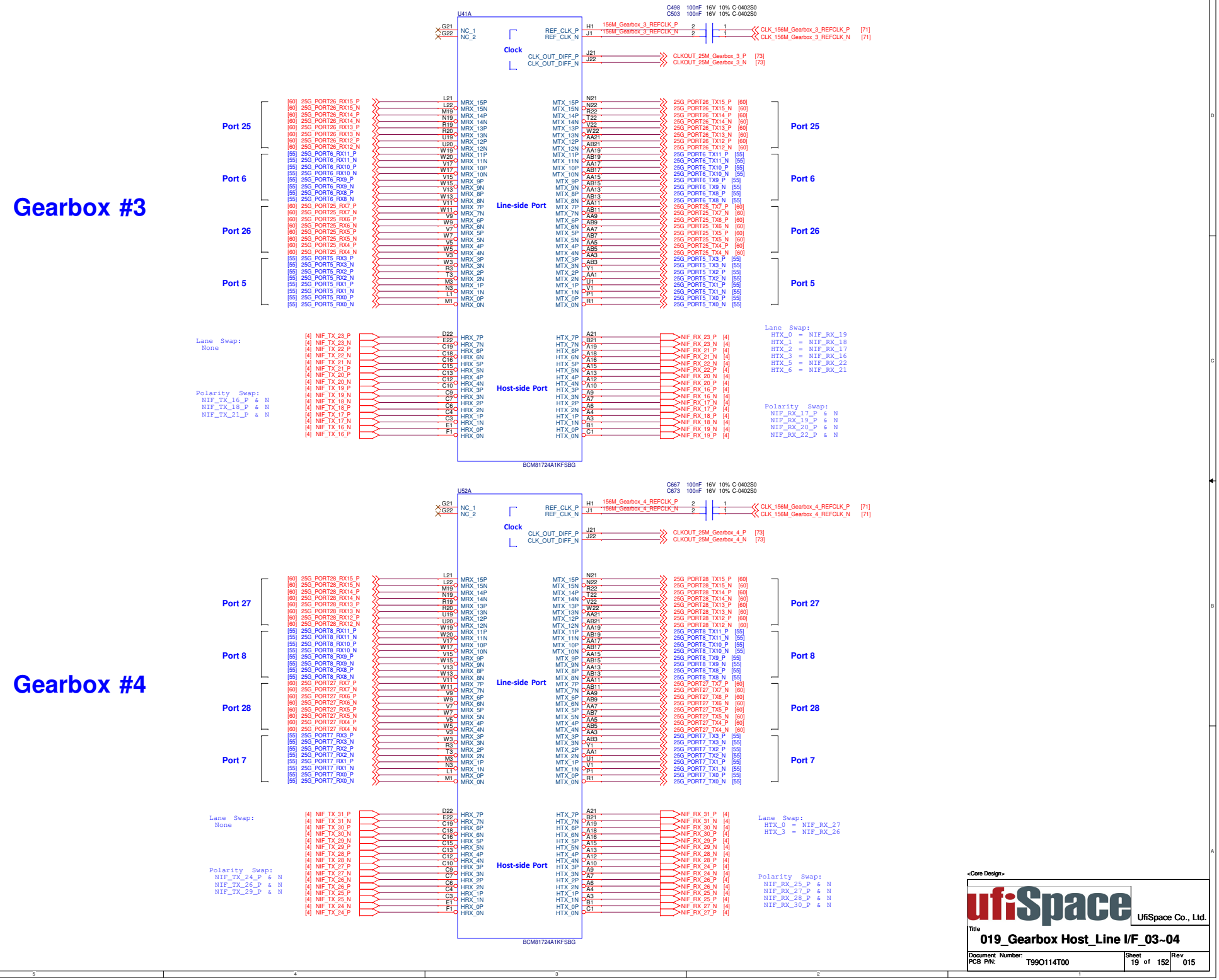
<Core Design>

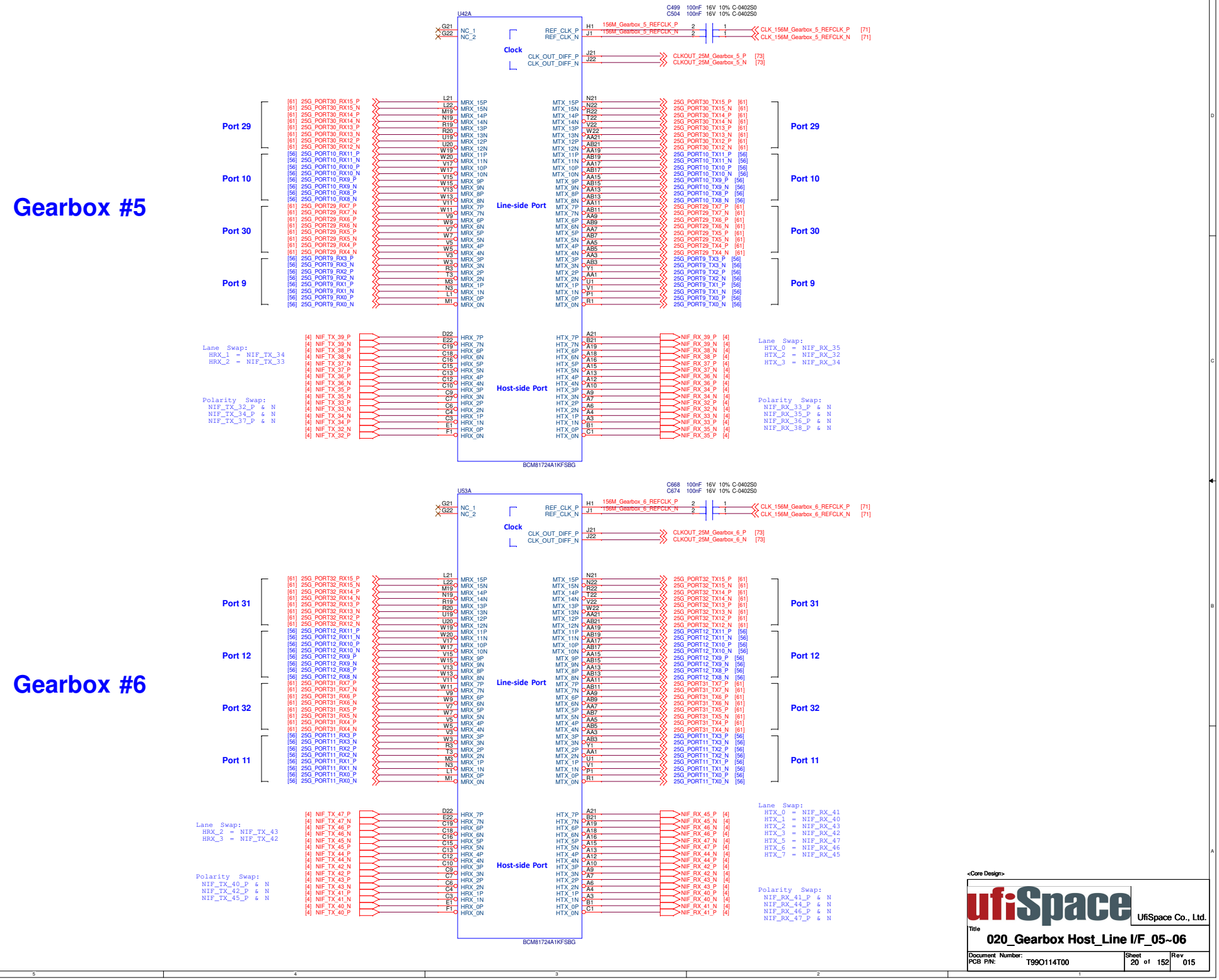
UfiSpace Co., Ltd.

Title

018_Gearbox Host_Line I/F_01~02

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	18 of 152	015


Gearbox #3
U41A
C498 100nF 16V 10% C-0402S0
C503 100nF 16V 10% C-0402S0
156M_Gearbox_3_REFCLK_P
156M_Gearbox_3_REFCLK_N
CLK_156M_Gearbox_3_REFCLK_P [71]
CLK_156M_Gearbox_3_REFCLK_N [71]
Clock
CLKOUT_25M_Gearbox_3_P [73]
CLKOUT_25M_Gearbox_3_N [73]
Port 25
Port 6
Port 26
Port 5
Line-side Port
Host-side Port
Lane Swap:
None
Polarity Swap:
NIF_TX_16_P & N
NIF_TX_18_P & N
NIF_TX_21_P & N
Lane Swap:
HTX_0 = NIF_RX_19
HTX_1 = NIF_RX_18
HTX_2 = NIF_RX_17
HTX_3 = NIF_RX_16
HTX_5 = NIF_RX_22
HTX_6 = NIF_RX_21
Polarity Swap:
NIF_RX_17_P & N
NIF_RX_19_P & N
NIF_RX_20_P & N
NIF_RX_22_P & N
BCM81724A1KFSBG
Gearbox #4
U52A
C667 100nF 16V 10% C-0402S0
C673 100nF 16V 10% C-0402S0
156M_Gearbox_4_REFCLK_P
156M_Gearbox_4_REFCLK_N
CLK_156M_Gearbox_4_REFCLK_P [71]
CLK_156M_Gearbox_4_REFCLK_N [71]
Clock
CLKOUT_25M_Gearbox_4_P [73]
CLKOUT_25M_Gearbox_4_N [73]
Port 27
Port 8
Port 28
Port 7
Line-side Port
Host-side Port
Lane Swap:
None
Polarity Swap:
NIF_TX_24_P & N
NIF_TX_26_P & N
NIF_TX_29_P & N
Lane Swap:
HTX_0 = NIF_RX_27
HTX_3 = NIF_RX_26
Polarity Swap:
NIF_RX_25_P & N
NIF_RX_27_P & N
NIF_RX_28_P & N
NIF_RX_30_P & N
BCM81724A1KFSBG
<Core Design>
UfiSpace Co., Ltd.
Title
019_Gearbox Host_Line I/F_03~04
Document Number:
PCB P/N: T99O114T00
Sheet 19 of 152
Rev 015



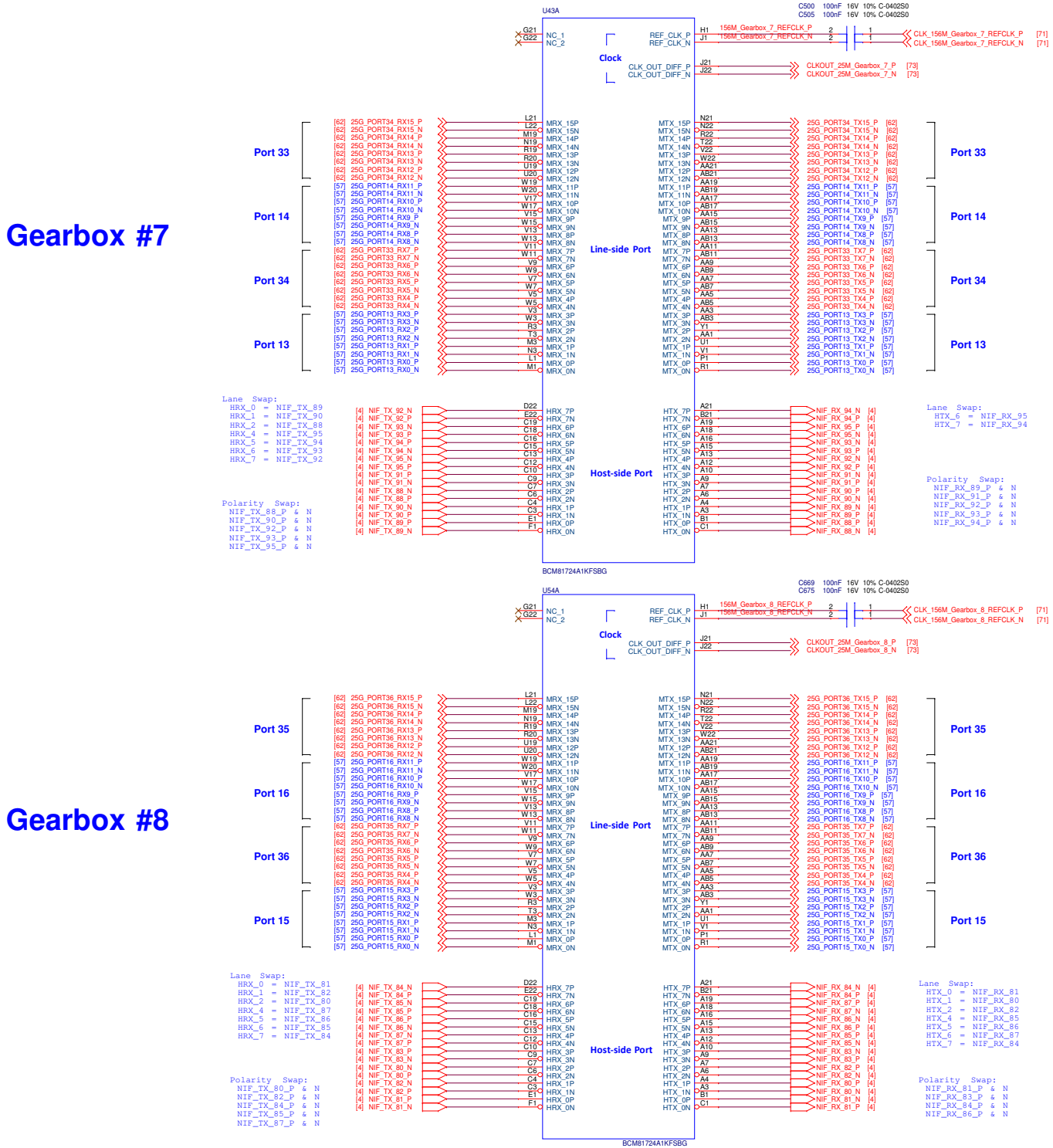
<Core Design>

UfiSpace Co., Ltd.

Title

020_Gearbox Host_Line I/F_05~06

Document Number: PCB P/N:	Sheet	Rev
T99O114T00	20 of 152	015



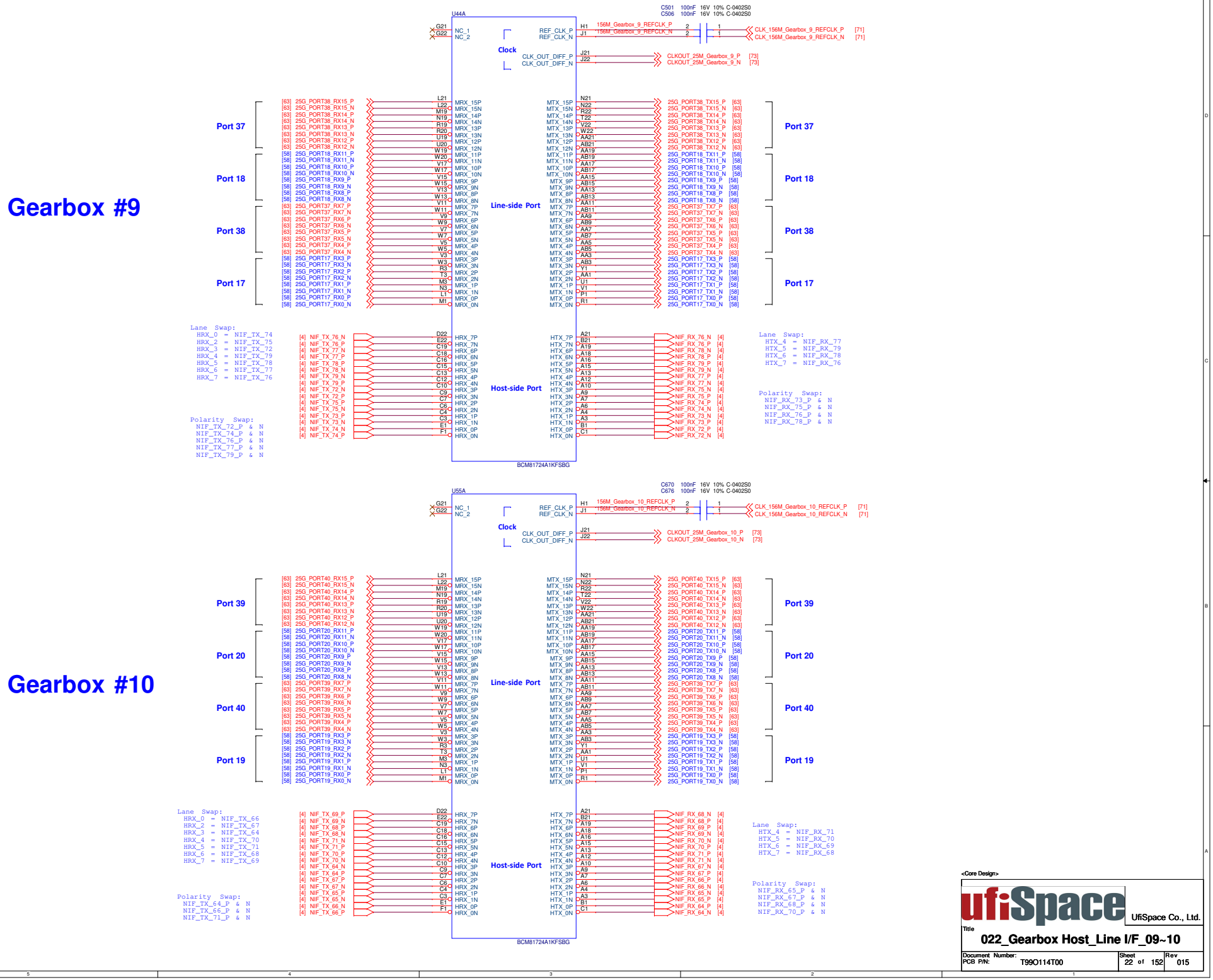
<Core Design>

UfiSpace Co., Ltd.

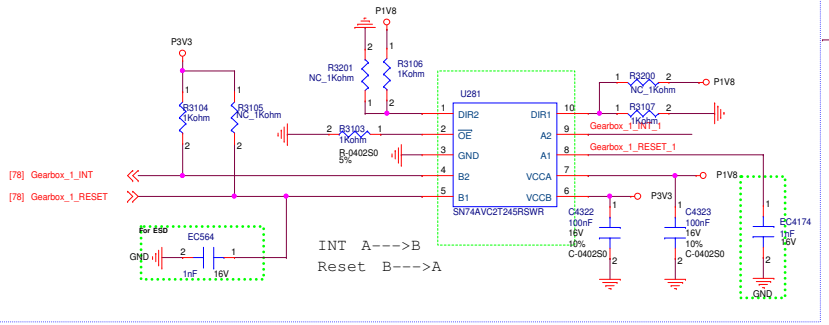
Title

021_Gearbox Host_Line I/F_07~08

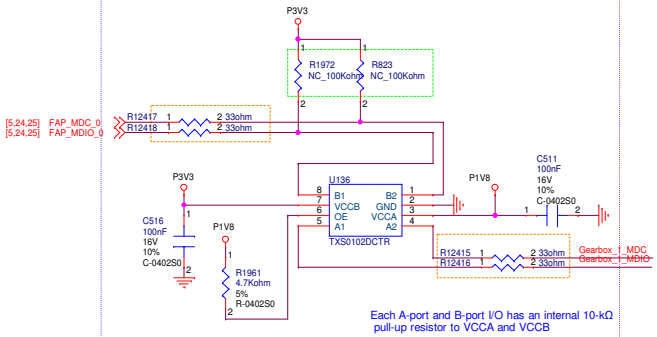
Document Number: PCB P/N: T99O114T00	Sheet 21 of 152	Rev 015


Gearbox #9
U44A
C501 100nF 16V 10% C-0402S0
C506 100nF 16V 10% C-0402S0
156M_Gearbox_9_REFCLK_P
156M_Gearbox_9_REFCLK_N
CLK_156M_Gearbox_9_REFCLK_P [71]
CLK_156M_Gearbox_9_REFCLK_N [71]
Clock
CLKOUT_25M_Gearbox_9_P [73]
CLKOUT_25M_Gearbox_9_N [73]
Port 37
Port 18
Port 38
Port 17
Line-side Port
Host-side Port
Lane Swap:
HRX_0 = NIF_TX_74
HRX_2 = NIF_TX_75
HRX_3 = NIF_TX_72
HRX_4 = NIF_TX_79
HRX_5 = NIF_TX_78
HRX_6 = NIF_TX_77
HRX_7 = NIF_TX_76
Polarity Swap:
NIF_TX_72_P & N
NIF_TX_74_P & N
NIF_TX_76_P & N
NIF_TX_77_P & N
NIF_TX_79_P & N
Lane Swap:
HTX_4 = NIF_RX_77
HTX_5 = NIF_RX_79
HTX_6 = NIF_RX_78
HTX_7 = NIF_RX_76
Polarity Swap:
NIF_RX_73_P & N
NIF_RX_75_P & N
NIF_RX_76_P & N
NIF_RX_78_P & N
BCM81724A1KFSBG
Gearbox #10
U55A
C670 100nF 16V 10% C-0402S0
C676 100nF 16V 10% C-0402S0
156M_Gearbox_10_REFCLK_P
156M_Gearbox_10_REFCLK_N
CLK_156M_Gearbox_10_REFCLK_P [71]
CLK_156M_Gearbox_10_REFCLK_N [71]
Clock
CLKOUT_25M_Gearbox_10_P [73]
CLKOUT_25M_Gearbox_10_N [73]
Port 39
Port 20
Port 40
Port 19
Line-side Port
Host-side Port
Lane Swap:
HRX_0 = NIF_TX_66
HRX_2 = NIF_TX_67
HRX_3 = NIF_TX_64
HRX_4 = NIF_TX_70
HRX_5 = NIF_TX_71
HRX_6 = NIF_TX_68
HRX_7 = NIF_TX_69
Polarity Swap:
NIF_TX_64_P & N
NIF_TX_66_P & N
NIF_TX_71_P & N
Lane Swap:
HTX_4 = NIF_RX_71
HTX_5 = NIF_RX_70
HTX_6 = NIF_RX_69
HTX_7 = NIF_RX_68
Polarity Swap:
NIF_RX_65_P & N
NIF_RX_67_P & N
NIF_RX_68_P & N
NIF_RX_70_P & N
BCM81724A1KFSBG
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
022_Gearbox Host_Line I/F_09~10
Document Number:
PCB P/N: T99O114T00
Sheet 22 of 152
Rev 015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO



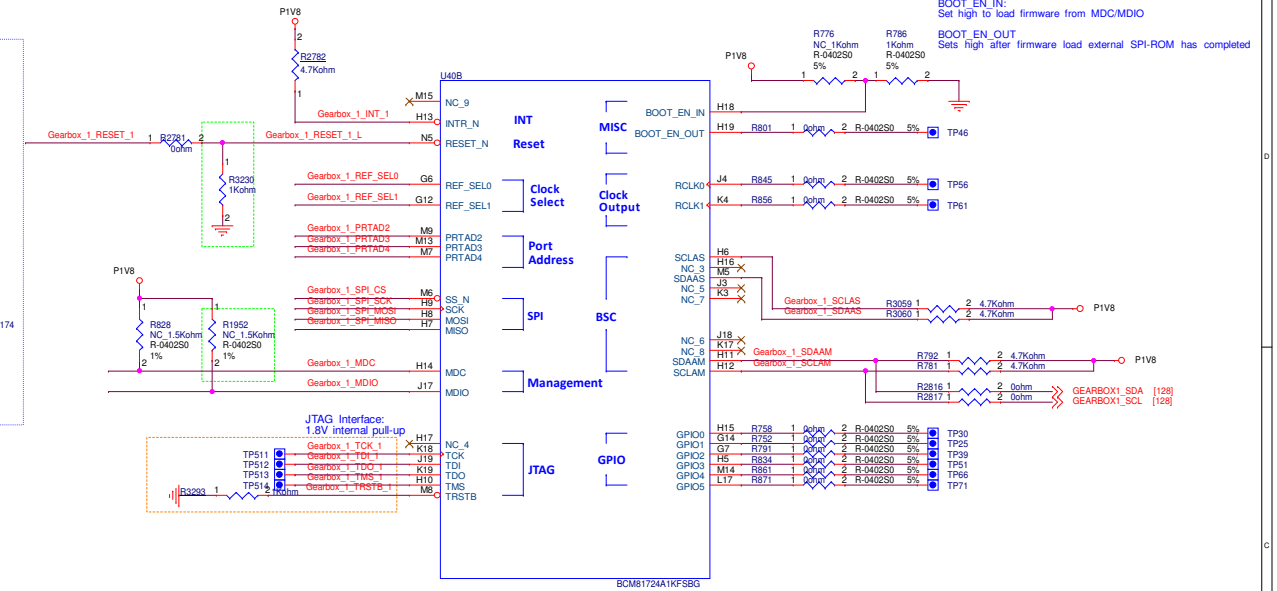
6.3 Recommended Operating Conditions

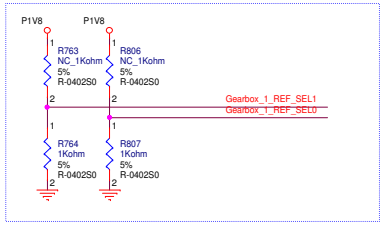
V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

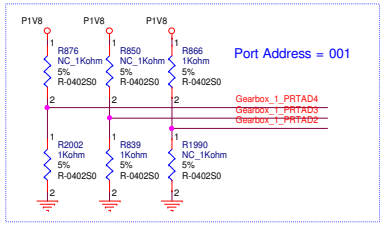
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

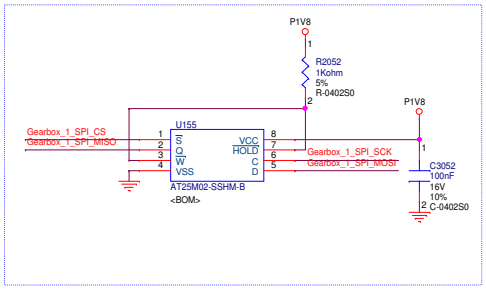
Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.









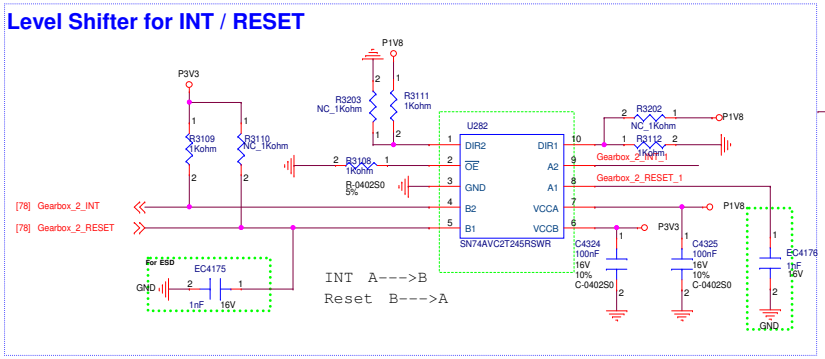
<Core Design>

ufiSpace UfiSpace Co., Ltd.

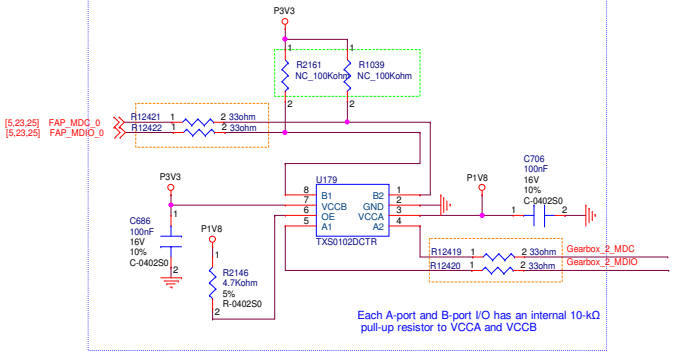
Title: 023_Gearbox RESET_MDIO_JTAG_01

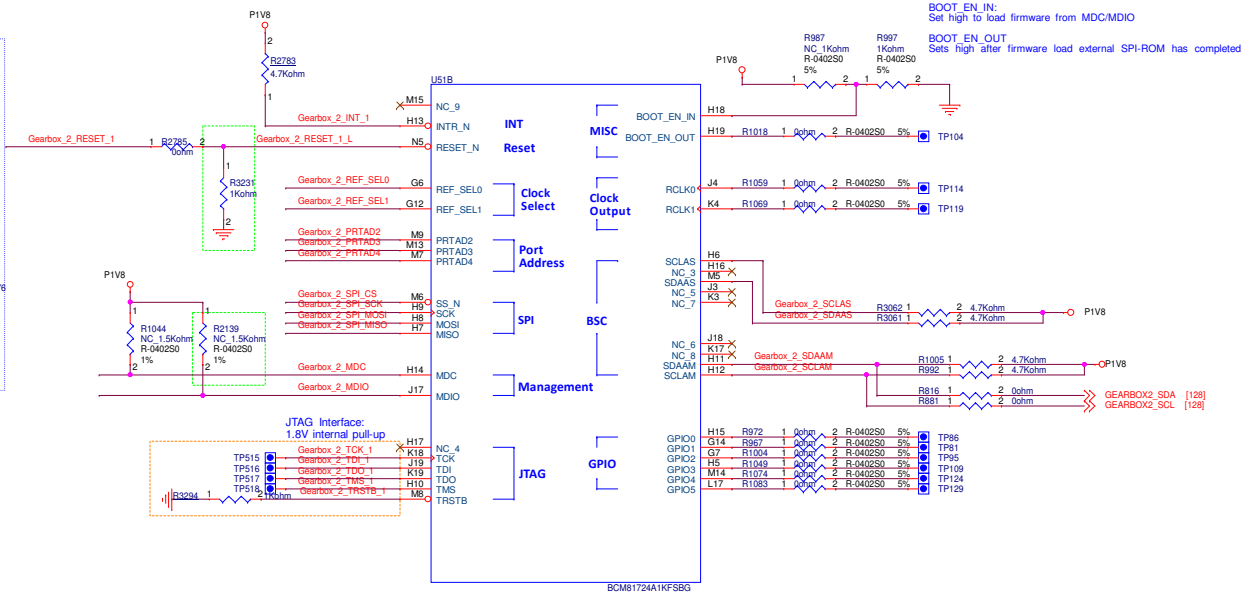
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	23 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





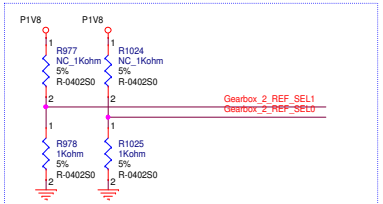
6.3 Recommended Operating Conditions

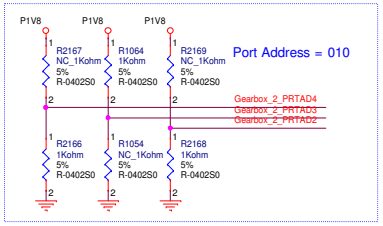
V_{CC} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

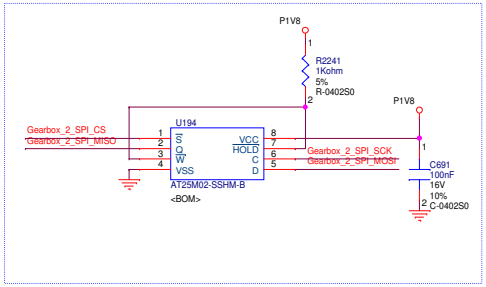
		MIN	MAX	UNIT
V_{CCA} Supply voltage[1]		1.65	3.6	V
V_{CCB} Supply voltage		2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







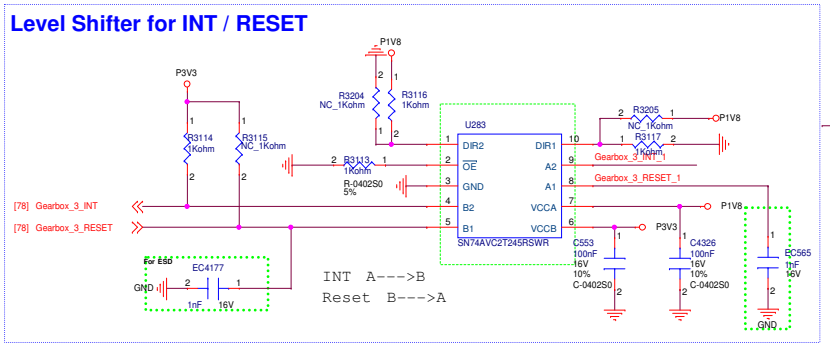
<Core Design>

ufiSpace UfiSpace Co., Ltd.

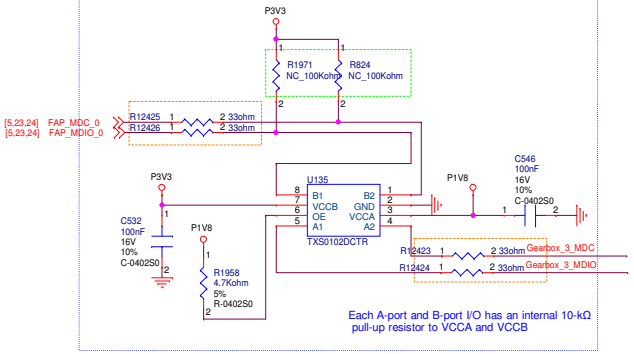
Title: 024_Gearbox RESET_MDIO_JTAG_02

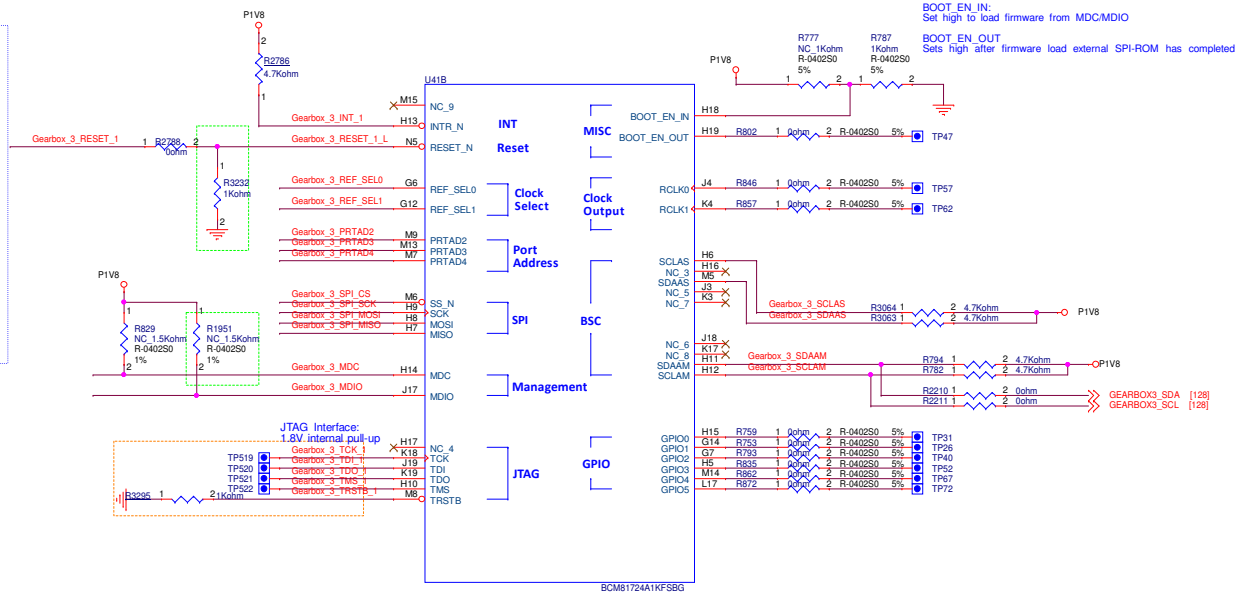
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	24 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





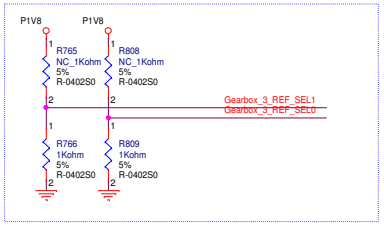
6.3 Recommended Operating Conditions

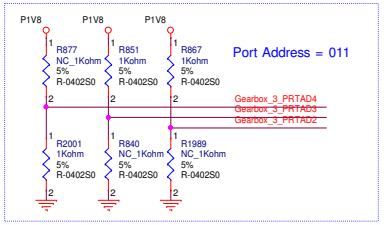
V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port

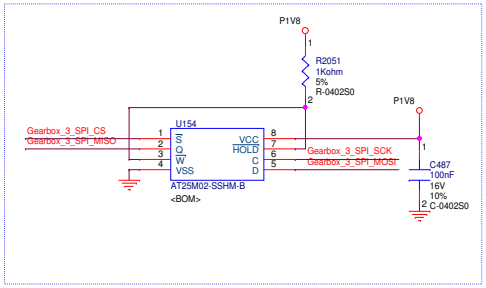
		MIN	MAX	UNIT
V_{CCA} Supply voltage[1]		1.65	3.6	V
V_{CCB} Supply voltage		2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







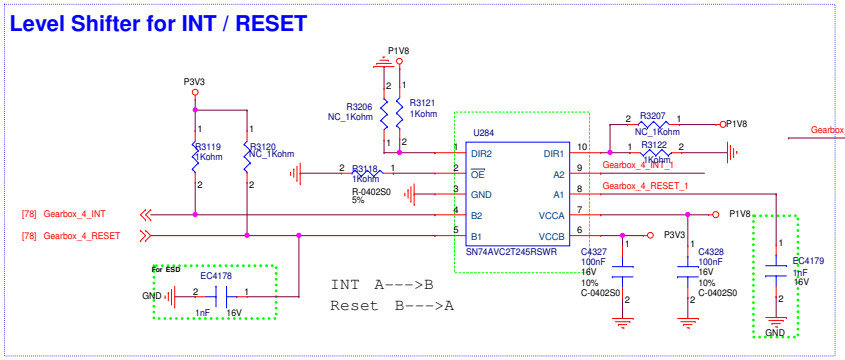
<Core Design>

UfiSpace Co., Ltd.

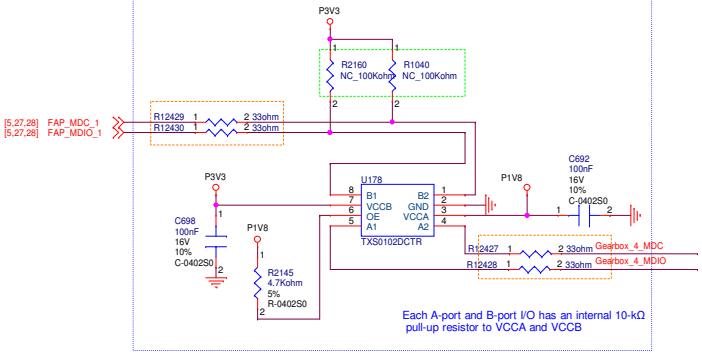
Title: 025_Gearbox RESET_MDIO_JTAG_03

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	25 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO



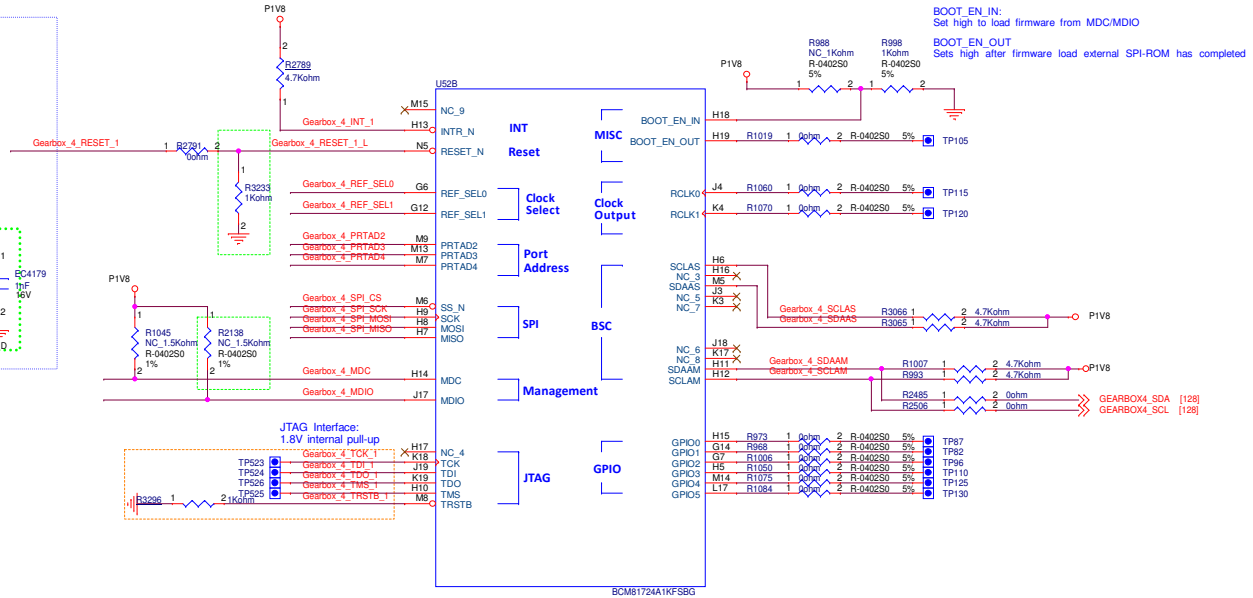
6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

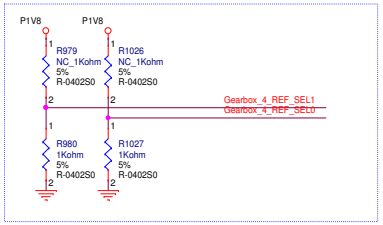
Note:

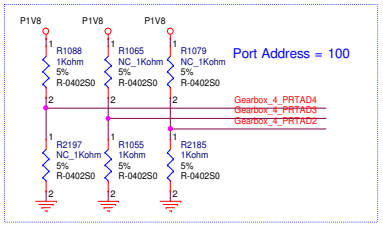
The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.

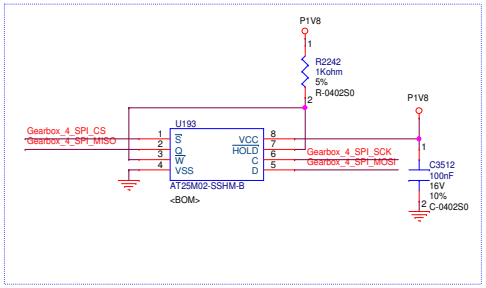


BOOT_EN_IN:
Set high to load firmware from MDC/MDIO

BOOT_EN_OUT
Sets high after firmware load external SPI-ROM has completed







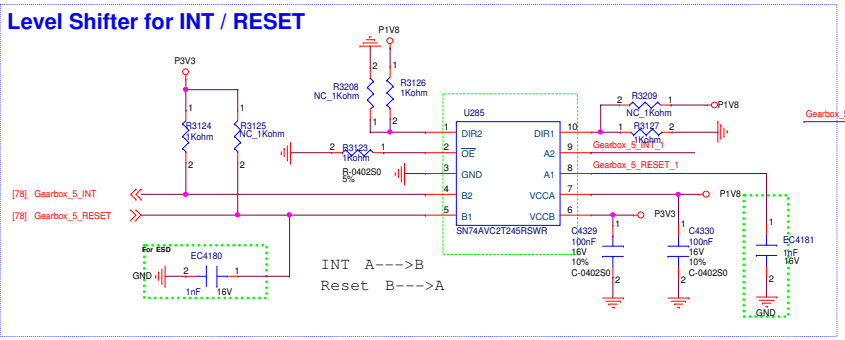
<Core Design>

UfiSpace Co., Ltd.

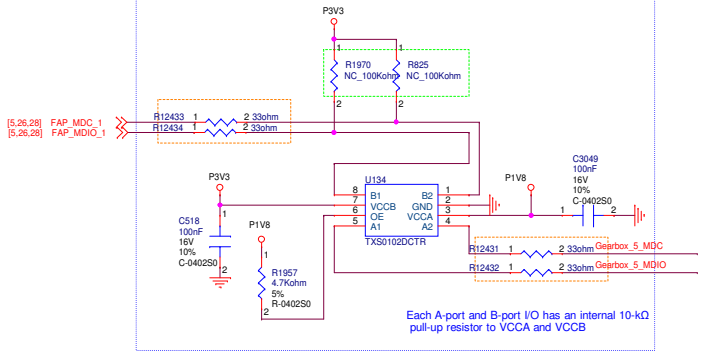
Title: 026_Gearbox RESET_MDIO_JTAG_04

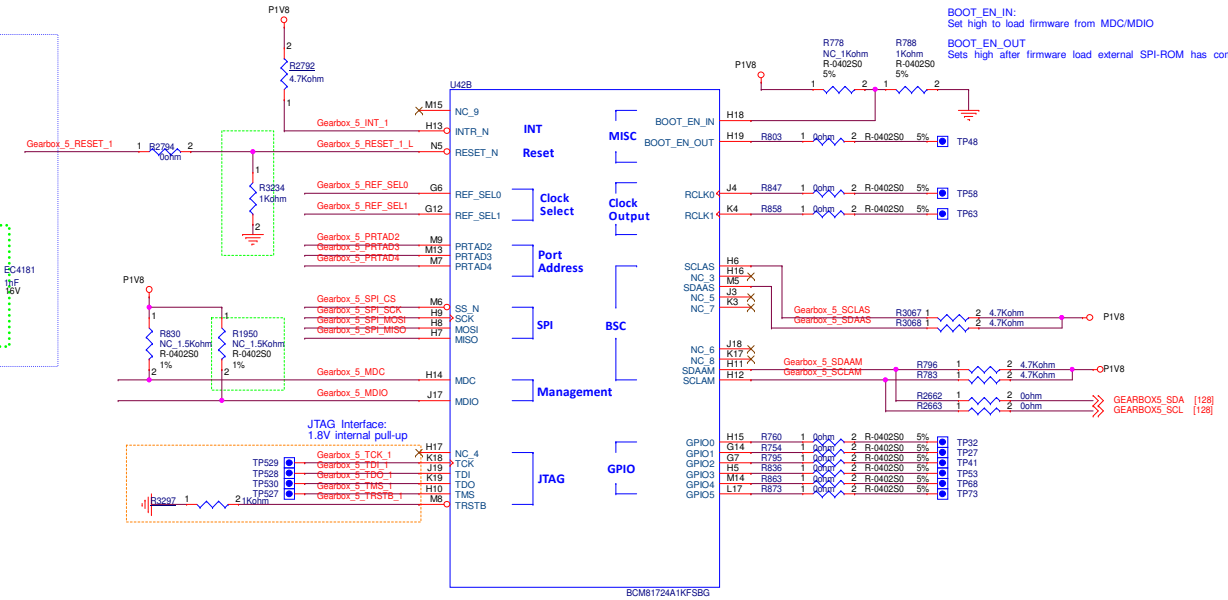
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	26 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





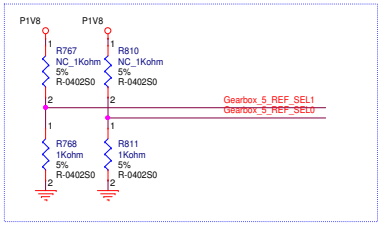
6.3 Recommended Operating Conditions

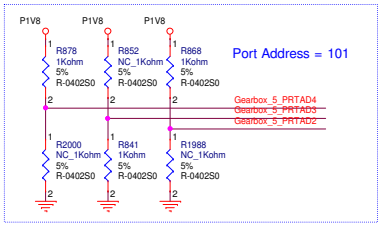
V_{CC} is the supply voltage associated with the input port. V_{CC} is the supply voltage associated with the output port.

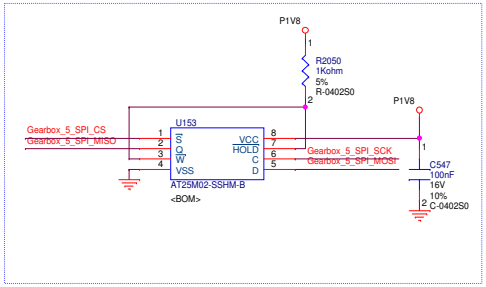
		MIN	MAX	UNIT
V_{CCA} Supply voltage[1]		1.65	3.6	V
V_{CCB} Supply voltage		2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







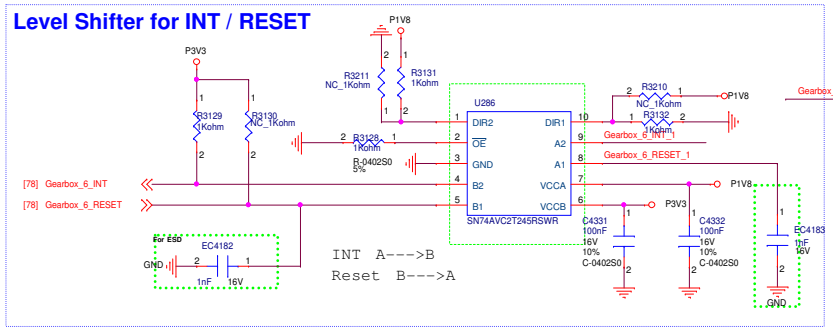
<Core Design>

UfiSpace Co., Ltd.

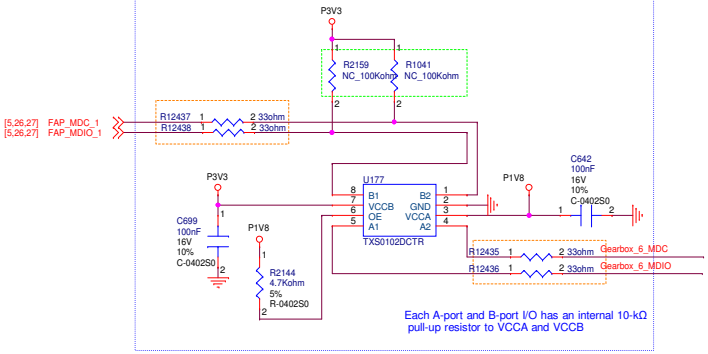
Title: 027_Gearbox RESET_MDIO_JTAG_05

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	27 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO



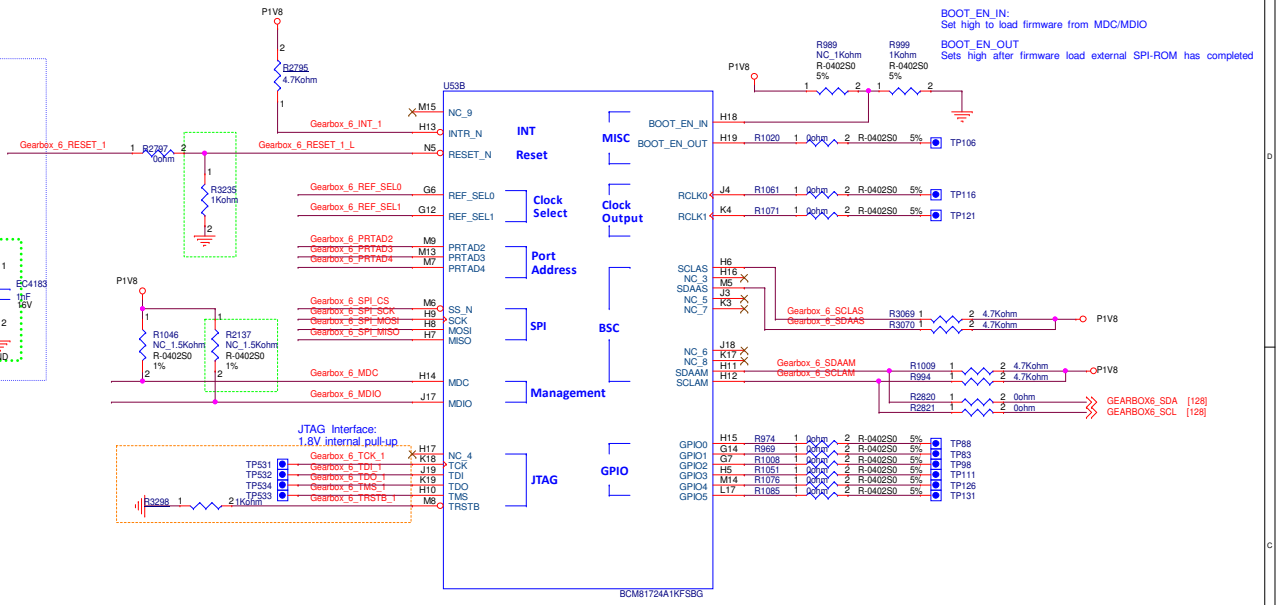
6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port, V_{CCO} is the supply voltage associated with the output port.

		MIN	MAX	UNIT
V_{CCA} Supply voltage[1]		1.65	3.6	V
V_{CCB} Supply voltage		2.3	5.5	V

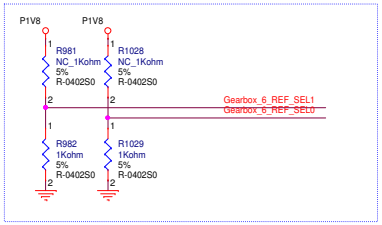
Note:

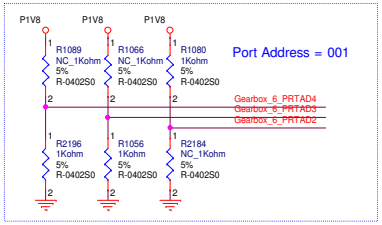
The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.

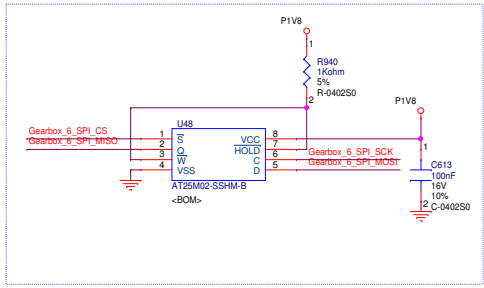


BOOT_EN_IN:
Set high to load firmware from MDC/MDIO

BOOT_EN_OUT
Sets high after firmware load external SPI-ROM has completed







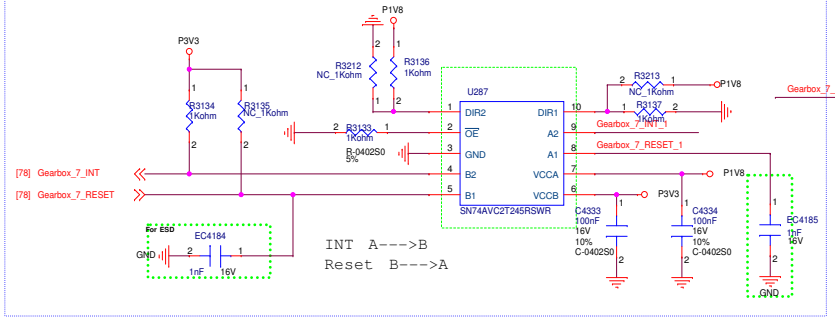
<Core Design>

UfiSpace Co., Ltd.

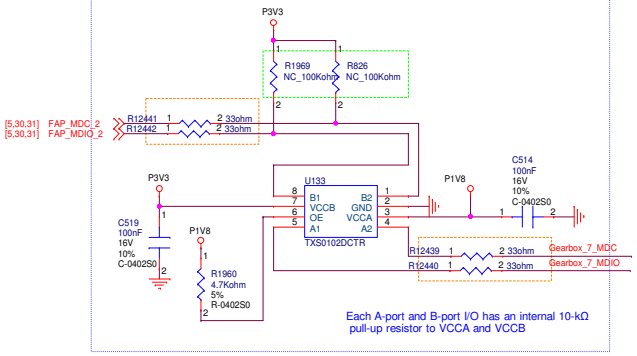
Title: 028_Gearbox RESET_MDIO_JTAG_06

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	28 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO



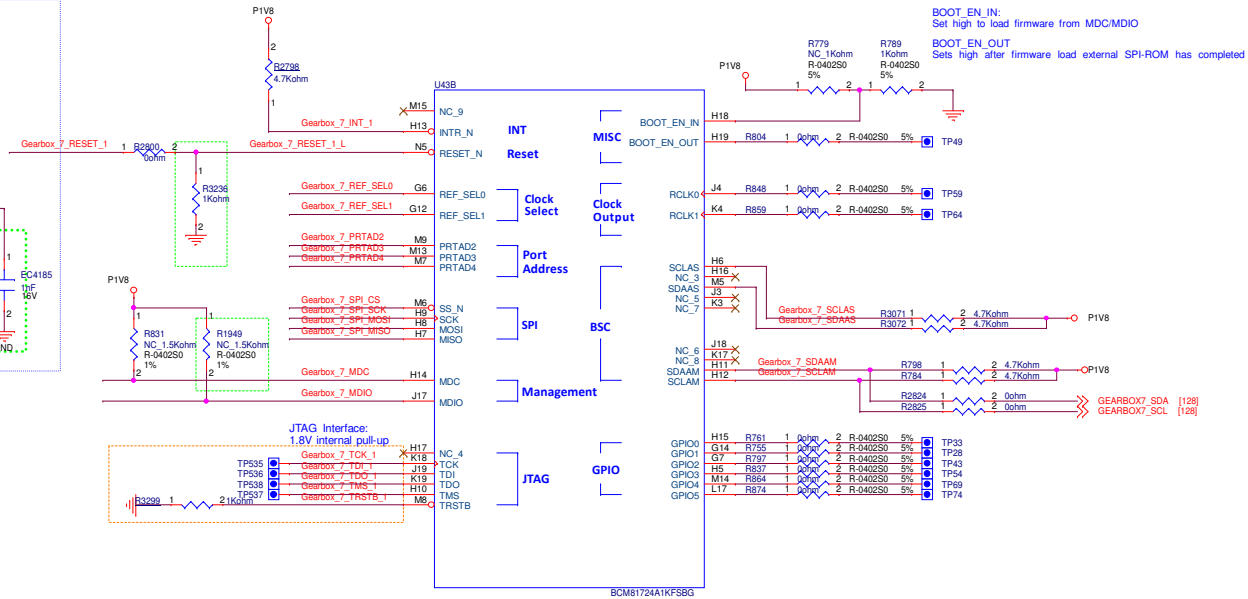
6.3 Recommended Operating Conditions

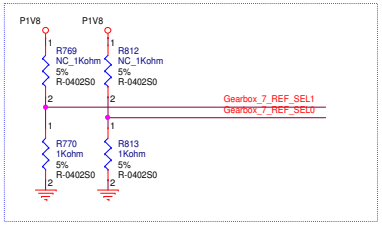
V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

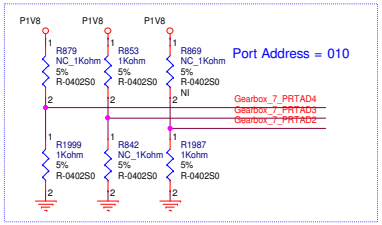
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

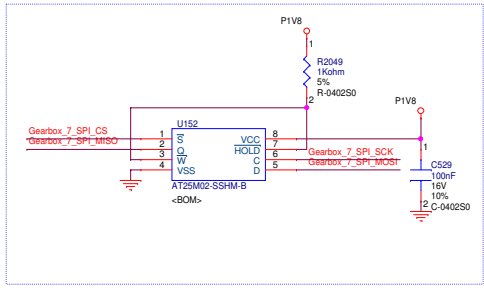
Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.









<Core Design>

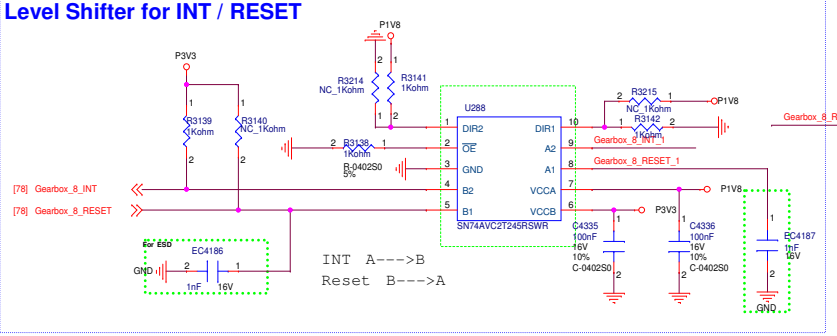
UfiSpace Co., Ltd.

Title

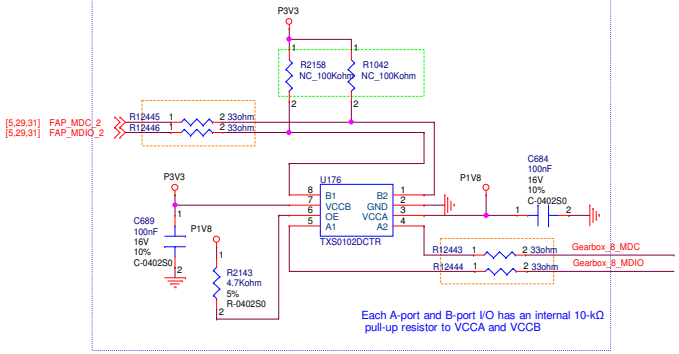
029_Gearbox RESET_MDIO_JTAG_07

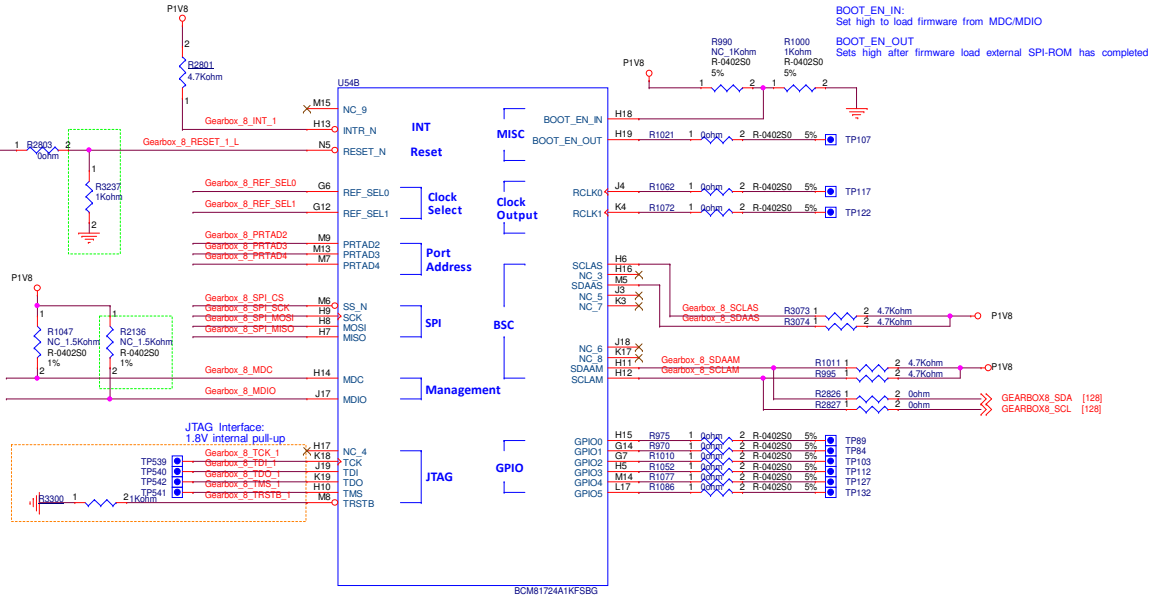
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	29 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





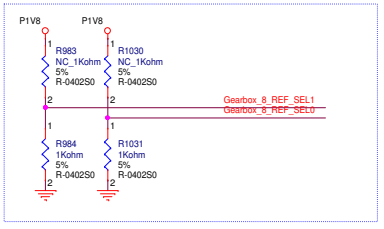
6.3 Recommended Operating Conditions

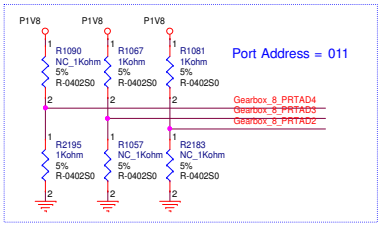
V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

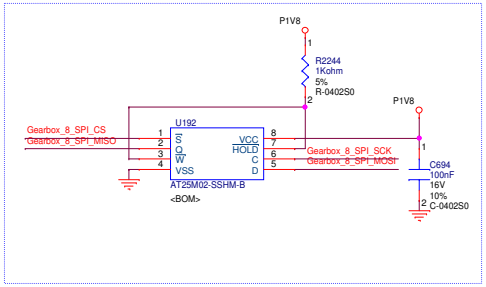
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







<Core Design>

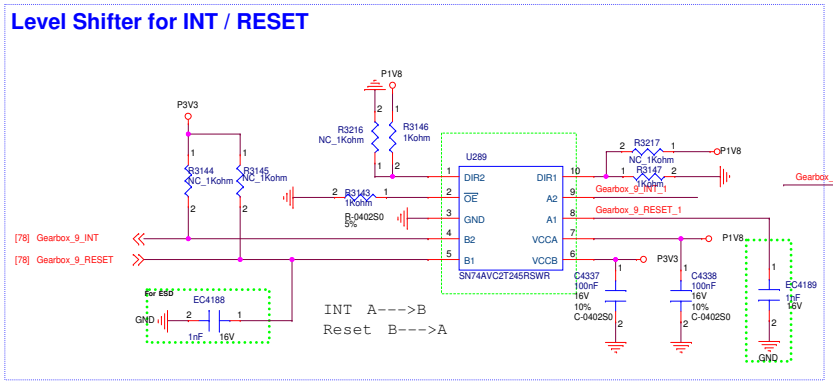
UfiSpace Co., Ltd.

Title

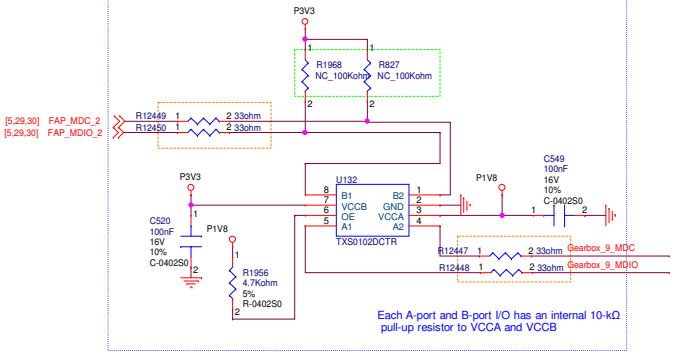
030_Gearbox RESET_MDIO_JTAG_08

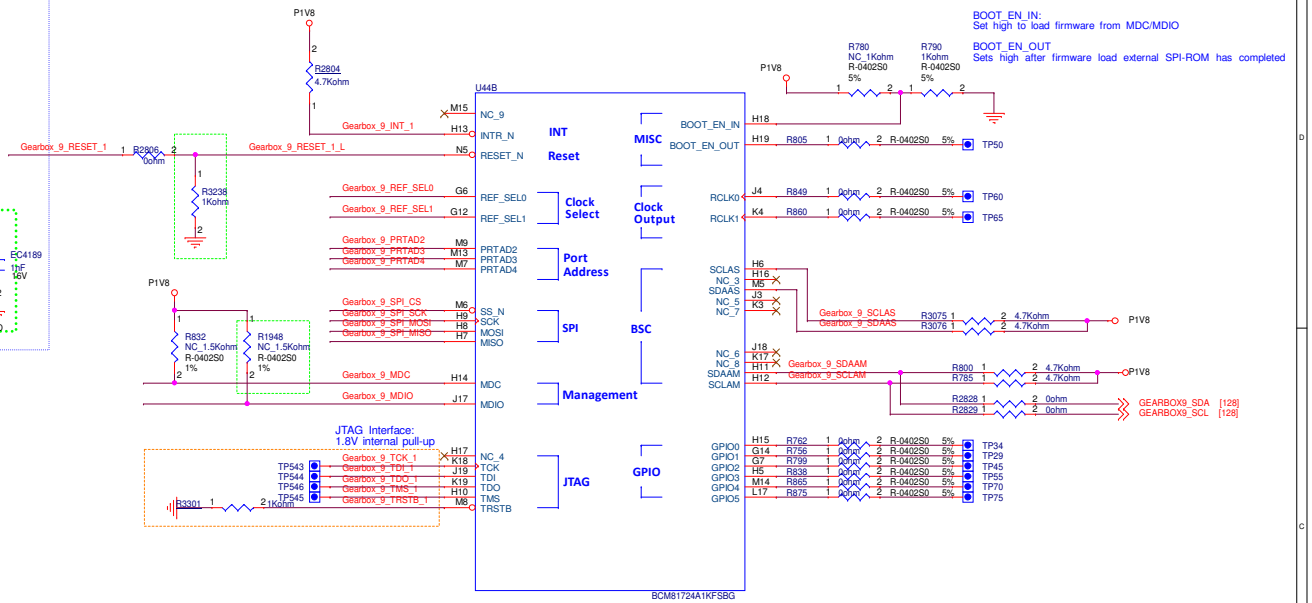
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	30 of 152	015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





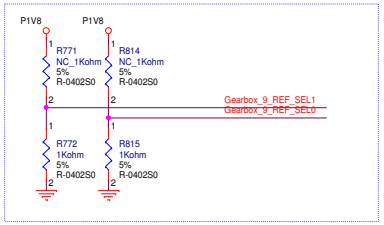
6.3 Recommended Operating Conditions

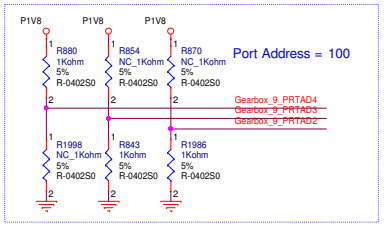
V_{CCI} is the supply voltage associated with the input port, V_{CCO} is the supply voltage associated with the output port

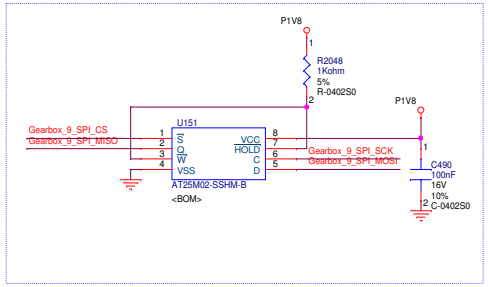
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







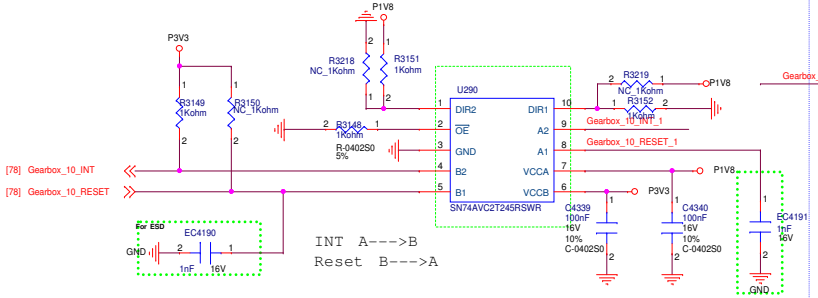
<Core Design>

ufiSpace UfiSpace Co., Ltd.

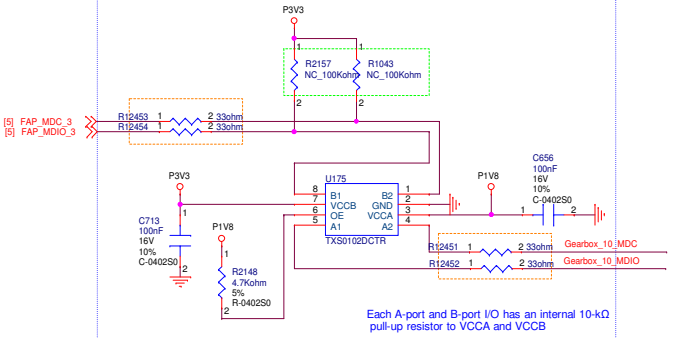
Title: 031_Gearbox RESET_MDIO_JTAG_09

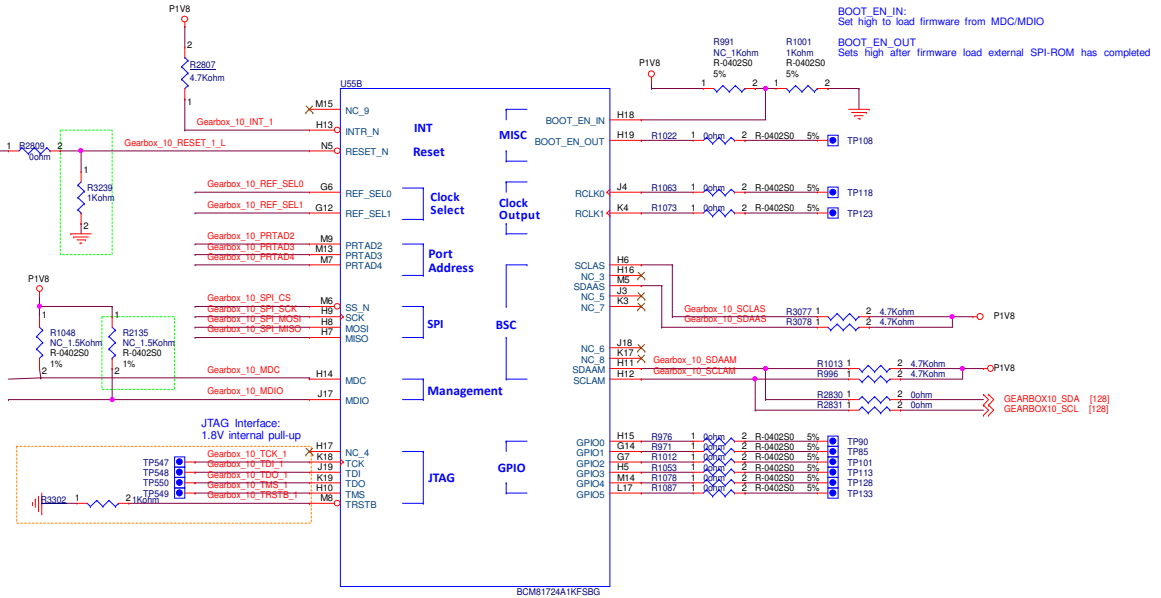
Document Number: PCB P/N: T99O114T00	Sheet 31 of 152	Rev 015

Level Shifter for INT / RESET



Level Shifter for MDC / MDIO





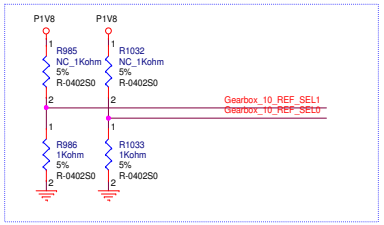
6.3 Recommended Operating Conditions

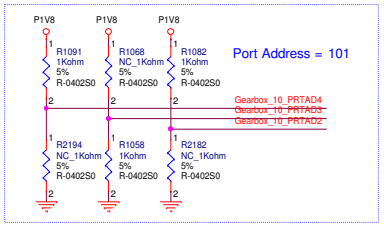
V_{CC} is the supply voltage associated with the input port, V_{CCO} is the supply voltage associated with the output port

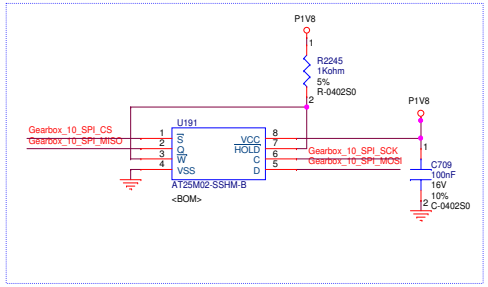
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.





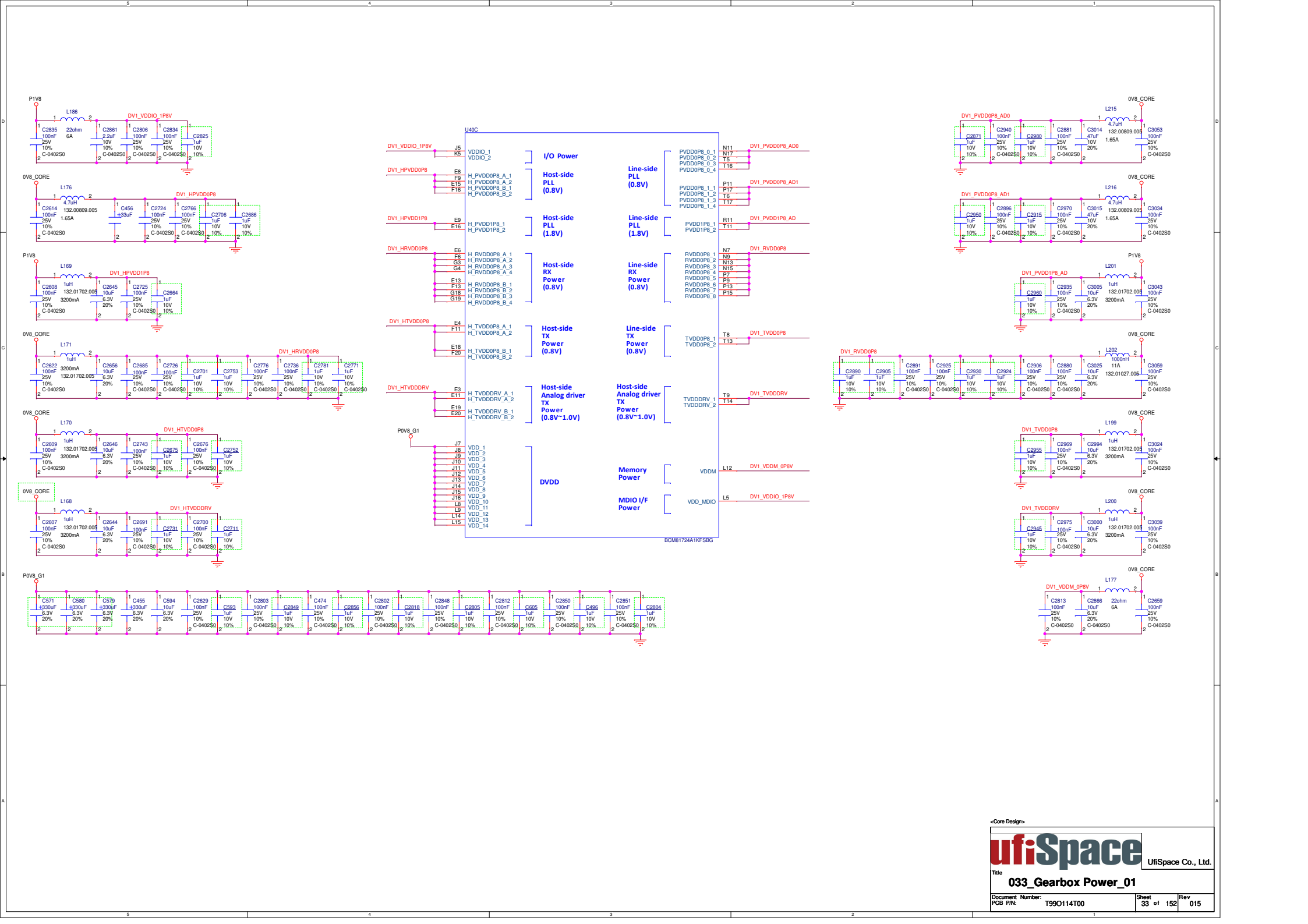


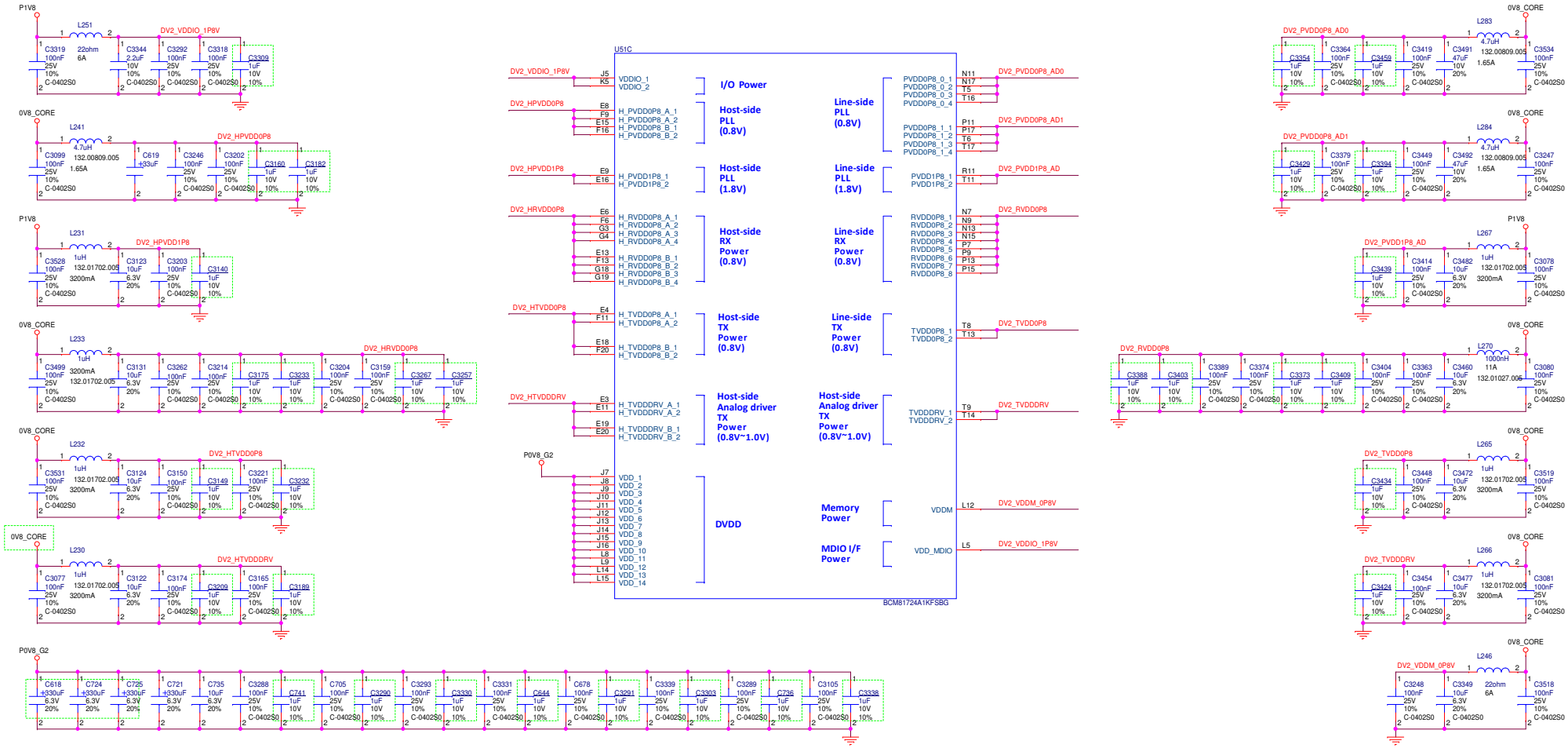
<Core Design>

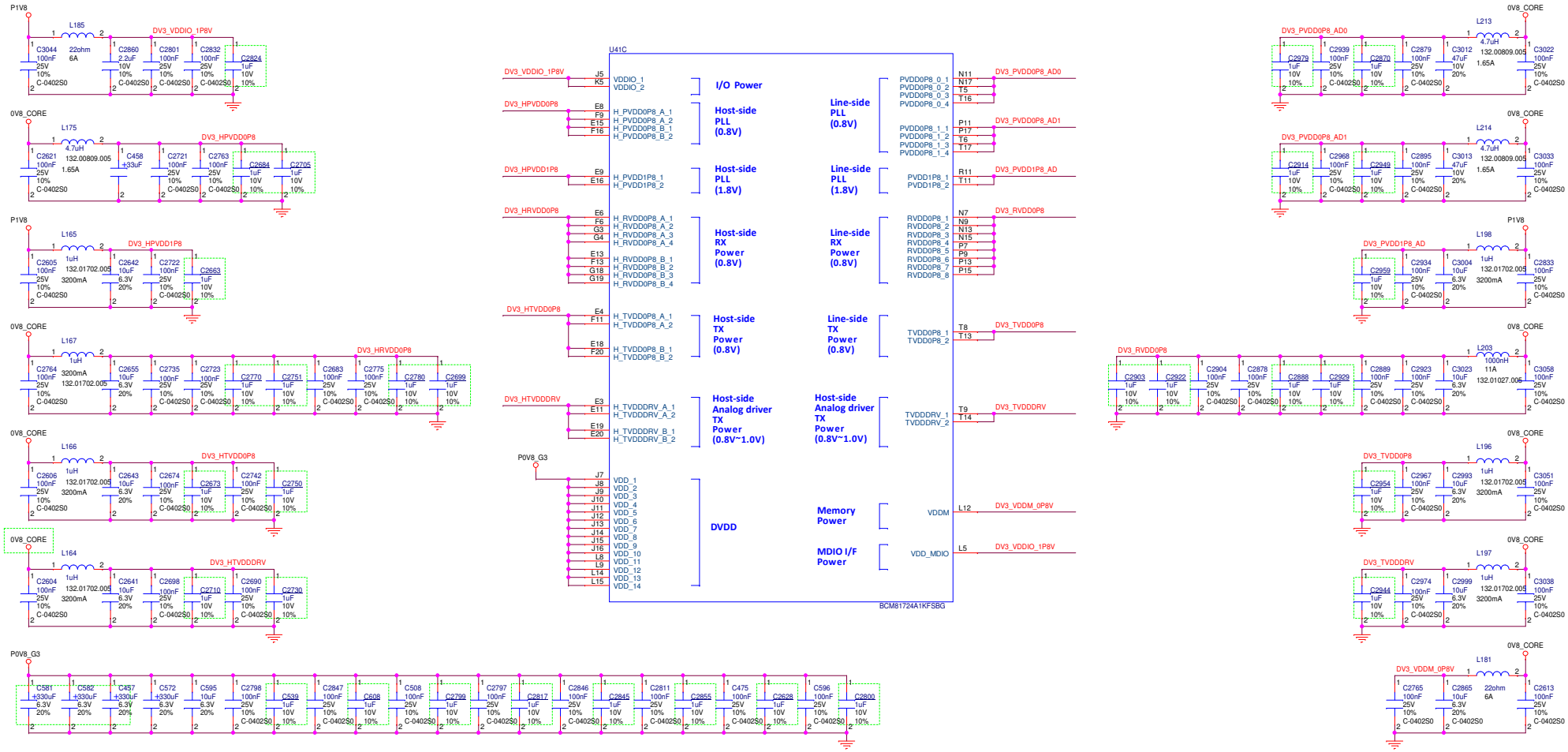
UfiSpace Co., Ltd.

Title: 032_Gearbox RESET_MDIO_JTAG_10

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	32 of 152	015


U40C
BCM81724A1KFSBG
I/O Power
Host-side PLL (0.8V)
Host-side PLL (1.8V)
Host-side RX Power (0.8V)
Host-side TX Power (0.8V)
Host-side Analog driver TX Power (0.8V~1.0V)
DVDD
Line-side PLL (0.8V)
Line-side PLL (1.8V)
Line-side RX Power (0.8V)
Line-side TX Power (0.8V)
Host-side Analog driver TX Power (0.8V~1.0V)
Memory Power
MDIO I/F Power
DV1_VDDIO_1P8V
DV1_HPVDD0P8
DV1_HPVDD1P8
DV1_HRVDD0P8
DV1_HTVDD0P8
DV1_HTVDDDRV
P0V8_G1
DV1_PVDD0P8_AD0
DV1_PVDD0P8_AD1
DV1_PVDD1P8_AD
DV1_RVDD0P8
DV1_TVDD0P8
DV1_TVDDDRV
DV1_VDDM_0P8V
DV1_VDDIO_1P8V
0V8_CORE
P1V8


U51C
BCM81724A1KFSBG
I/O Power
Host-side PLL (0.8V)
Host-side PLL (1.8V)
Host-side RX Power (0.8V)
Host-side TX Power (0.8V)
Host-side Analog driver TX Power (0.8V~1.0V)
DVDD
Line-side PLL (0.8V)
Line-side PLL (1.8V)
Line-side RX Power (0.8V)
Line-side TX Power (0.8V)
Host-side Analog driver TX Power (0.8V~1.0V)
Memory Power
MDIO I/F Power
DV2_VDDIO_1P8V
DV2_HPVDD0P8
DV2_HPVDD1P8
DV2_HRVDD0P8
DV2_HTVDD0P8
DV2_HTVDDDRV
P0V8_G2
DV2_PVDD0P8_AD0
DV2_PVDD0P8_AD1
DV2_PVDD1P8_AD
DV2_RVDD0P8
DV2_TVDD0P8
DV2_TVDDDRV
DV2_VDDM_0P8V
DV2_VDDIO_1P8V
0V8_CORE
P1V8

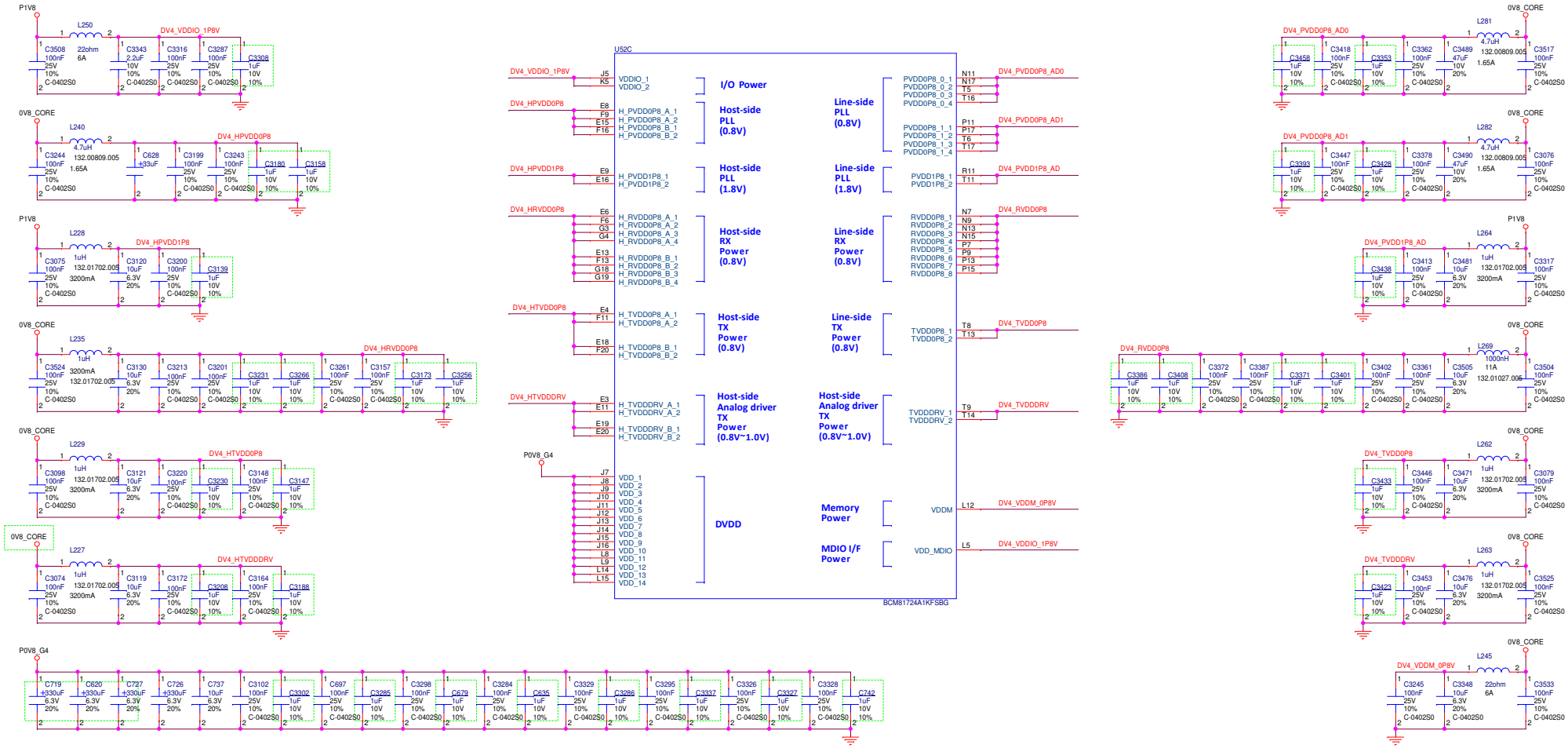


<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title: 035_Gearbox Power_03

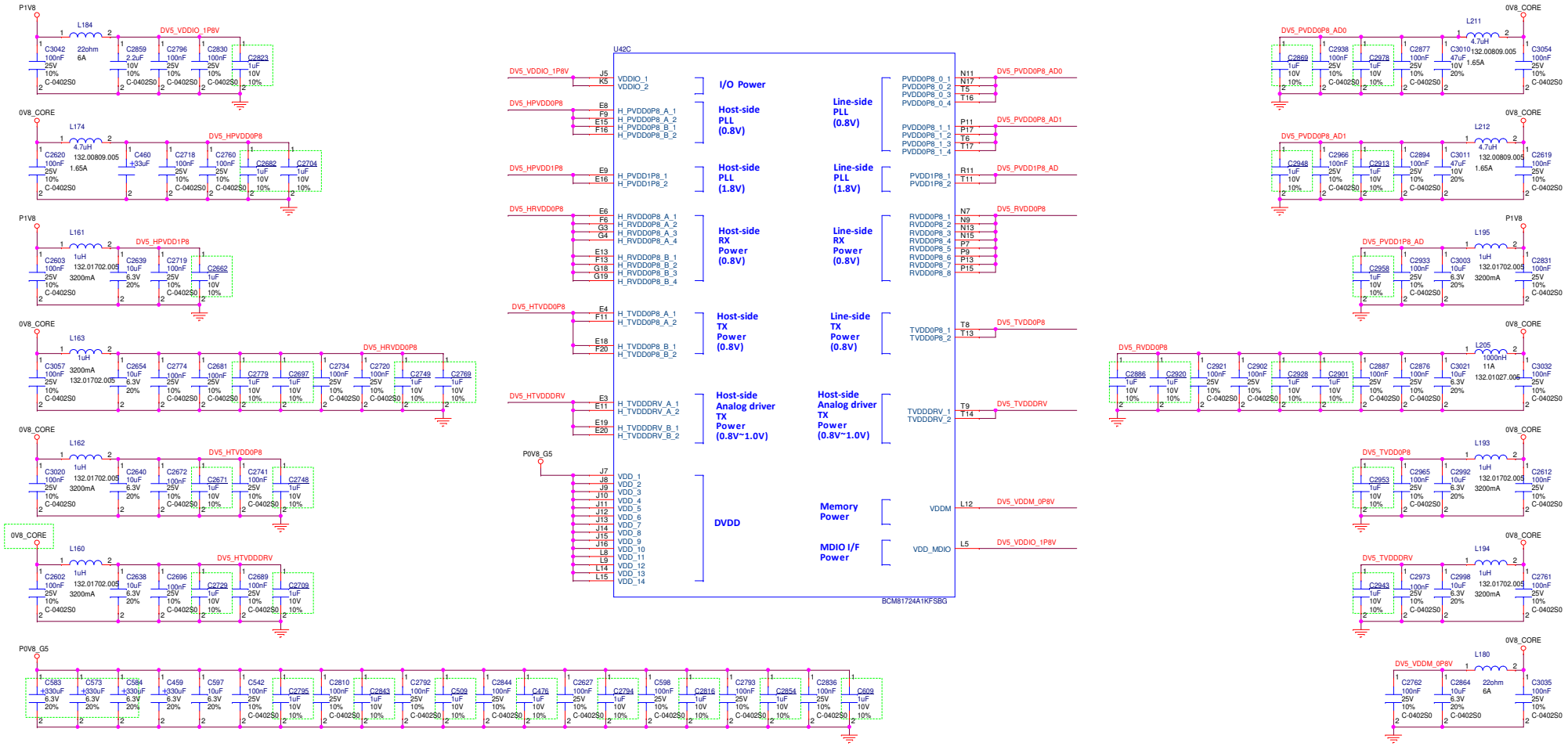
Document Number:	Sheet	Rev
PCB P/N: T99O114T00	35 of 152	015



<Core Design>
UfiSpace Co., Ltd.

Title
036_Gearbox Power_04

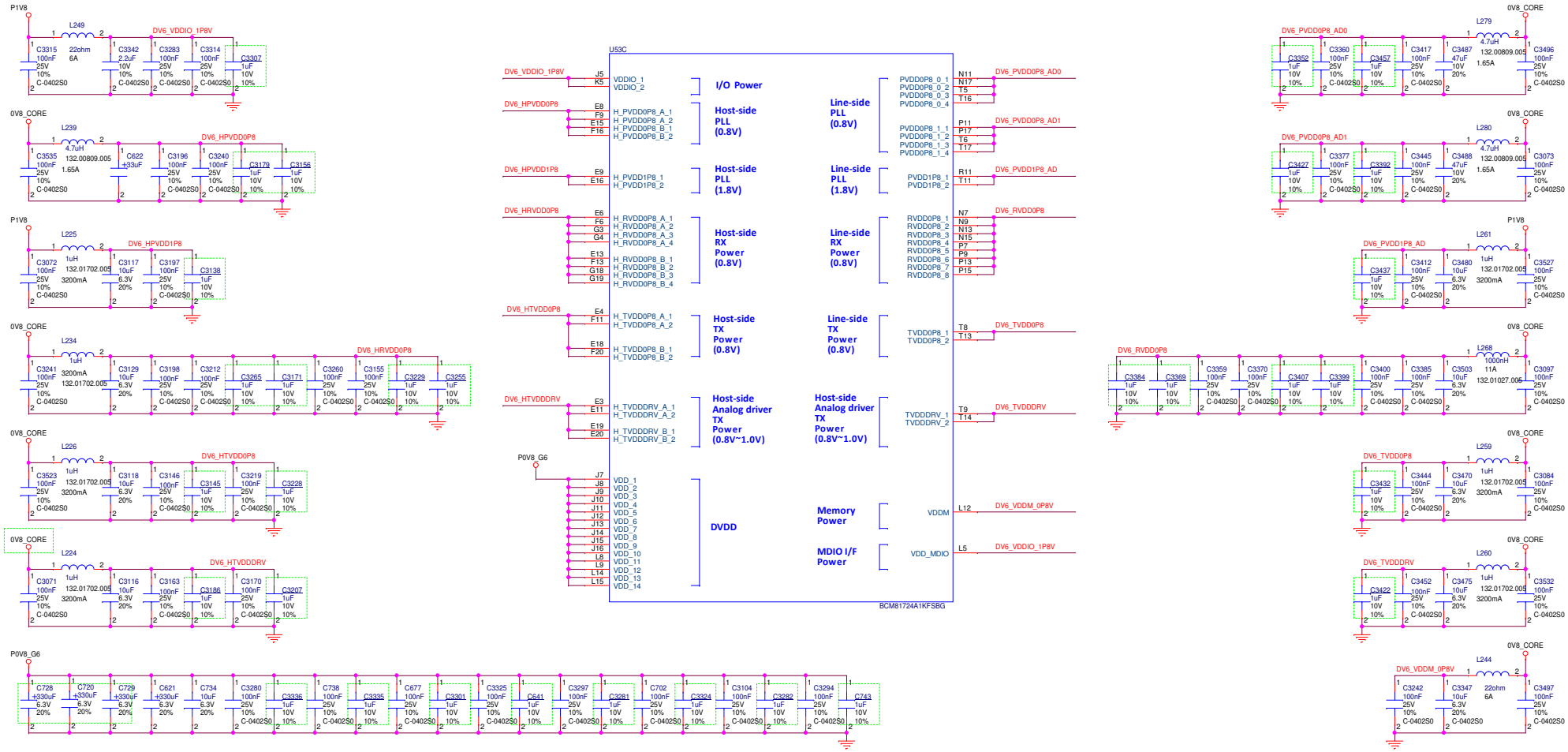
Document Number:	Sheet	Rev
PCB P/N: T99O114T00	36 of 152	015



<Core Design>
UfiSpace Co., Ltd.

Title
037_Gearbox Power_05

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	37 of 152	015



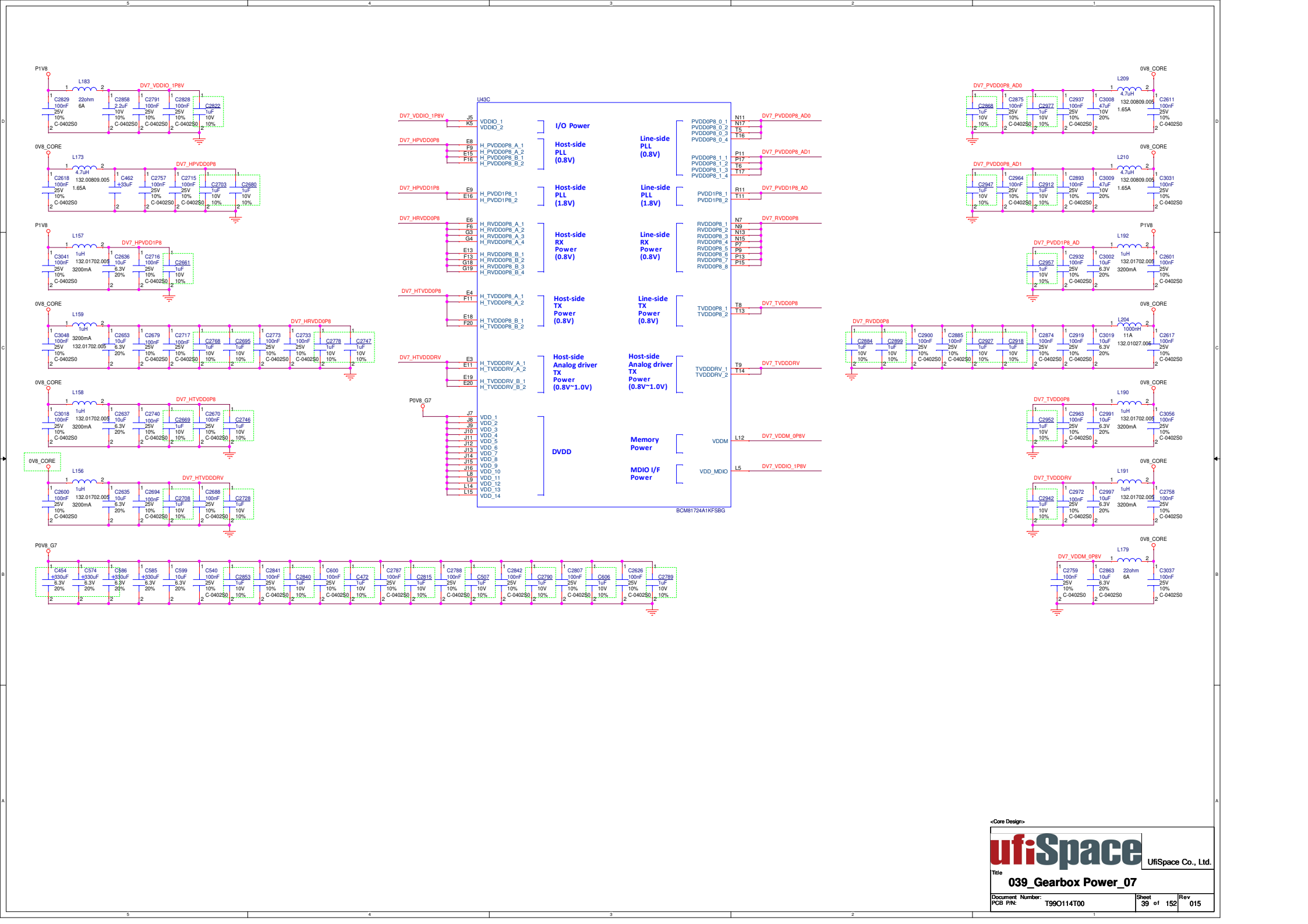
<Core Design>

UfiSpace Co., Ltd.

Title

038_Gearbox Power_06

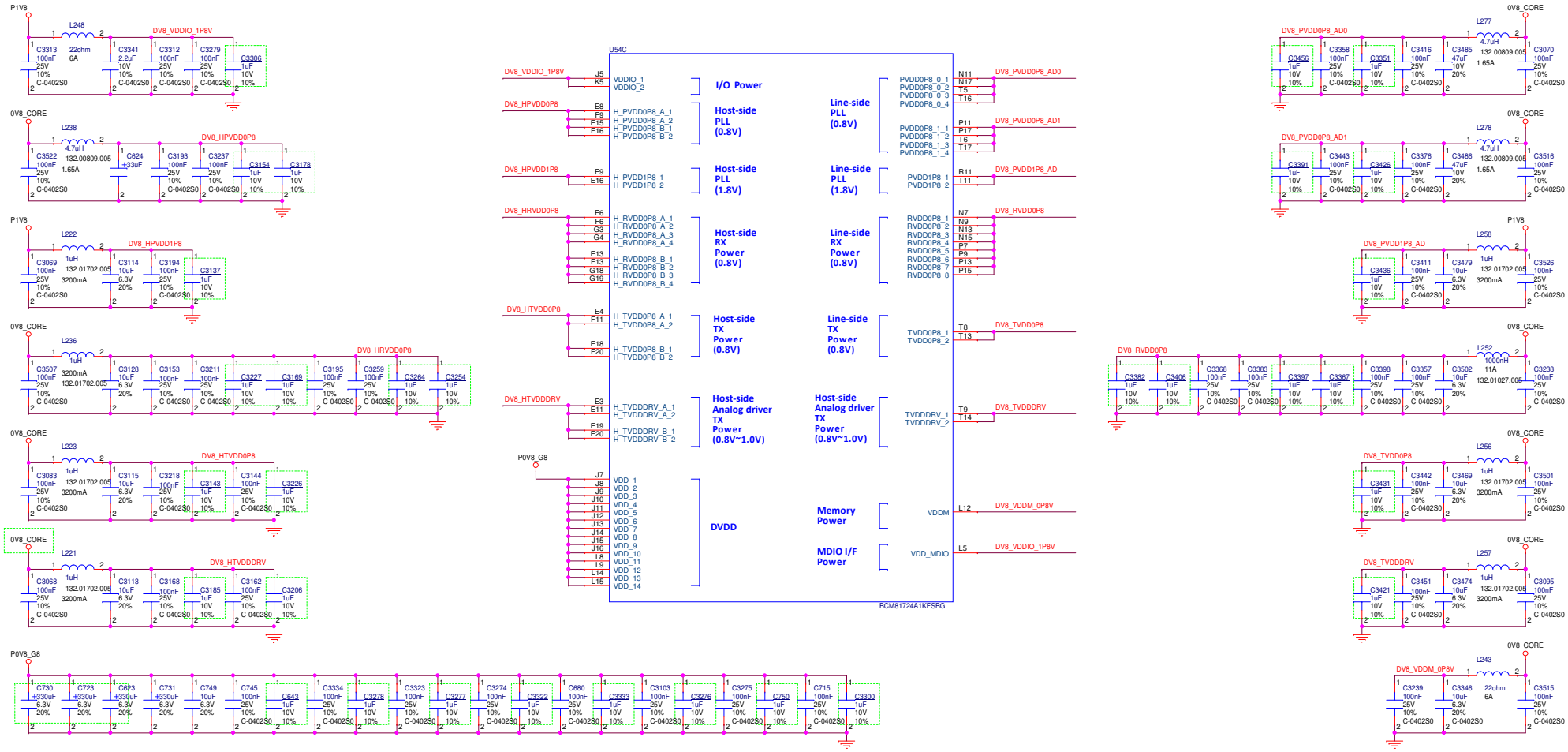
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	38 of 152	015



<Core Design>
UfiSpace Co., Ltd.

Title: 039_Gearbox Power_07

Document Number: T99O114T00
PCB P/N:
Sheet 39 of 152
Rev 015



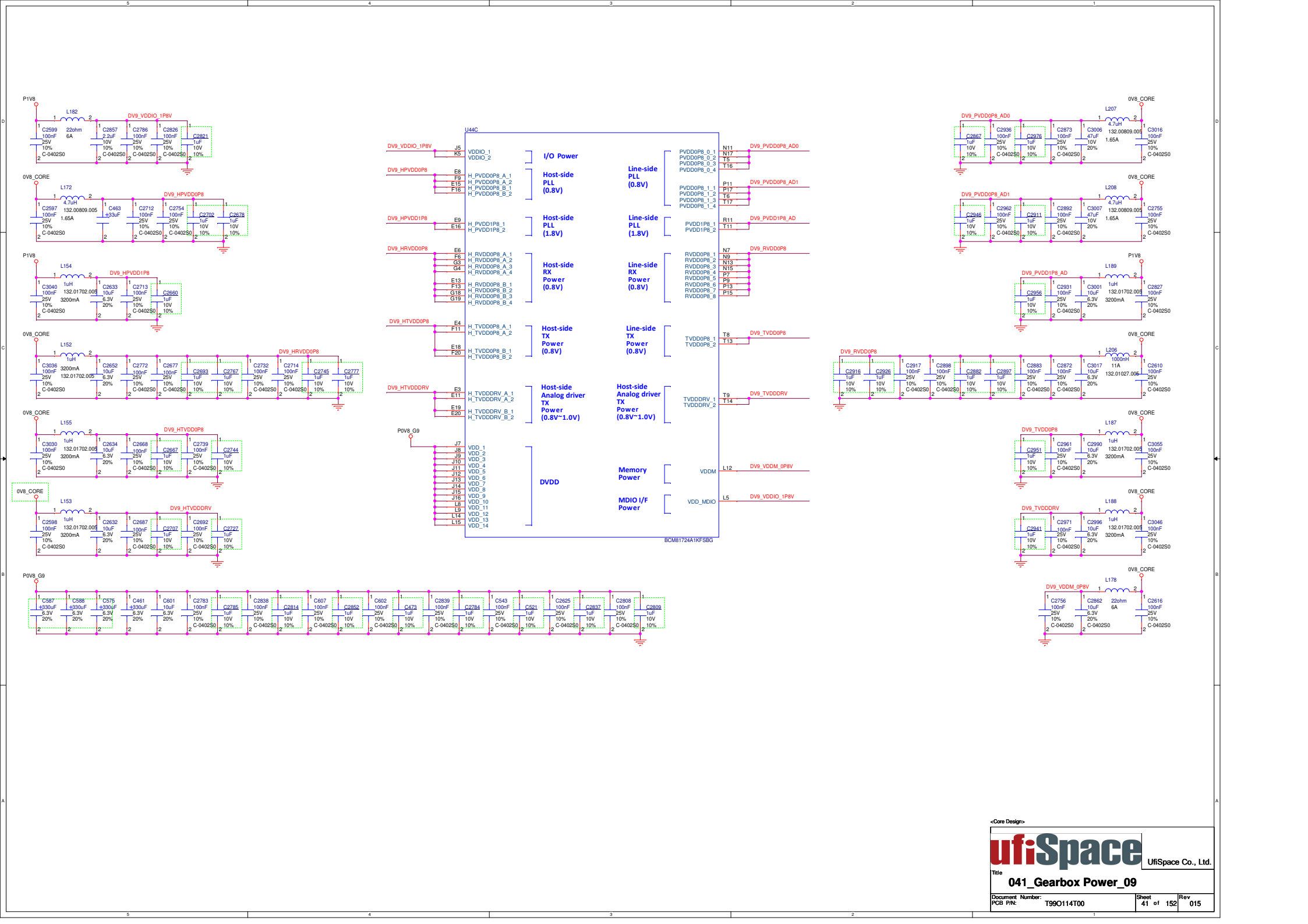
<Core Design>

UfiSpace Co., Ltd.

Title

040_Gearbox Power_08

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	40 of 152	015

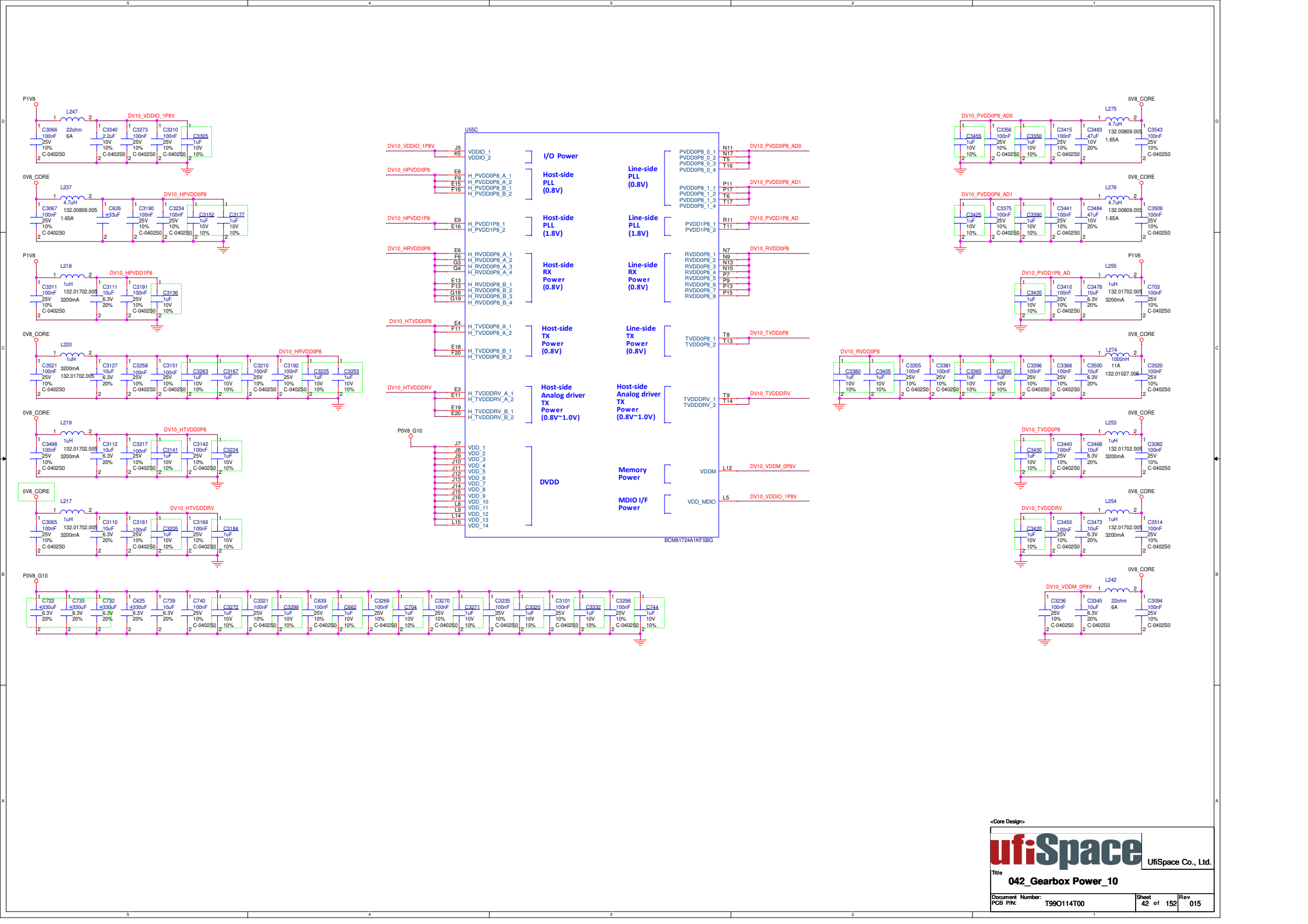


<Core Design>

UfiSpace Co., Ltd.

Title: 041_Gearbox Power_09

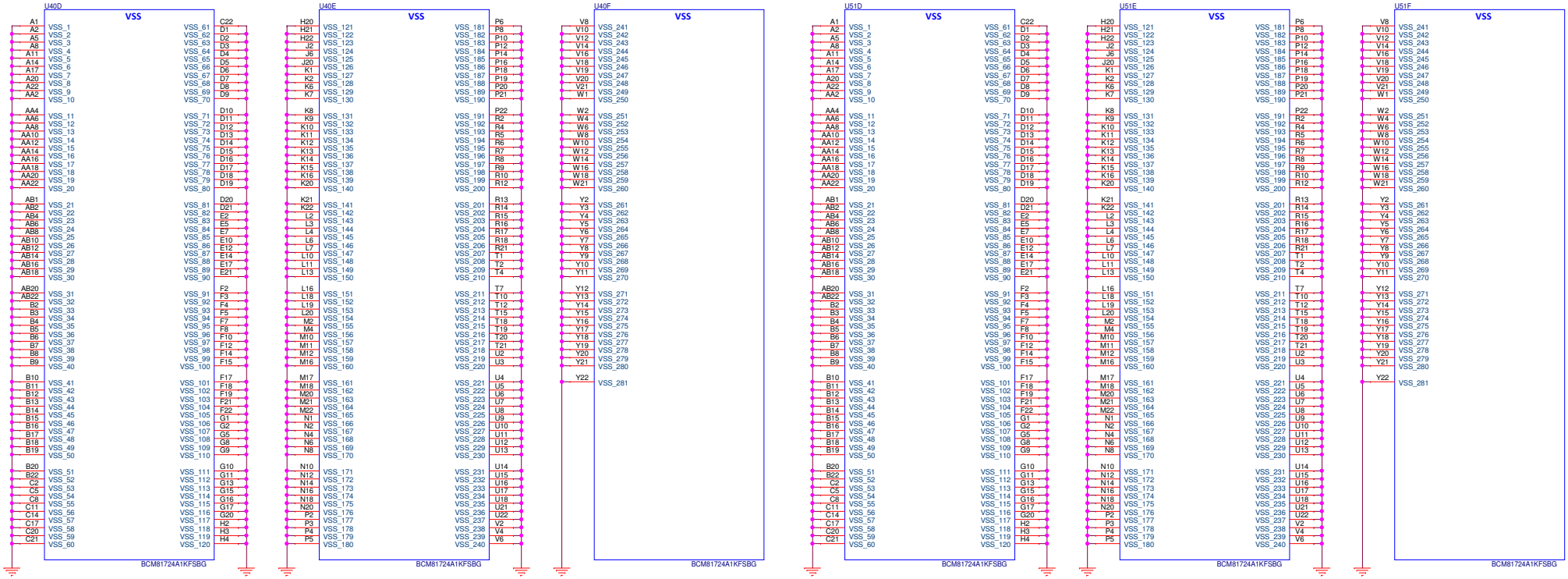
Document Number:	Sheet	Rev
PCB P/N: T99O114T00	41 of 152	015



<Core Design>
UfiSpace Co., Ltd.

Title
042_Gearbox Power_10

Document Number:		Sheet	Rev
PCB P/N: T99O114T00		42 of 152	015



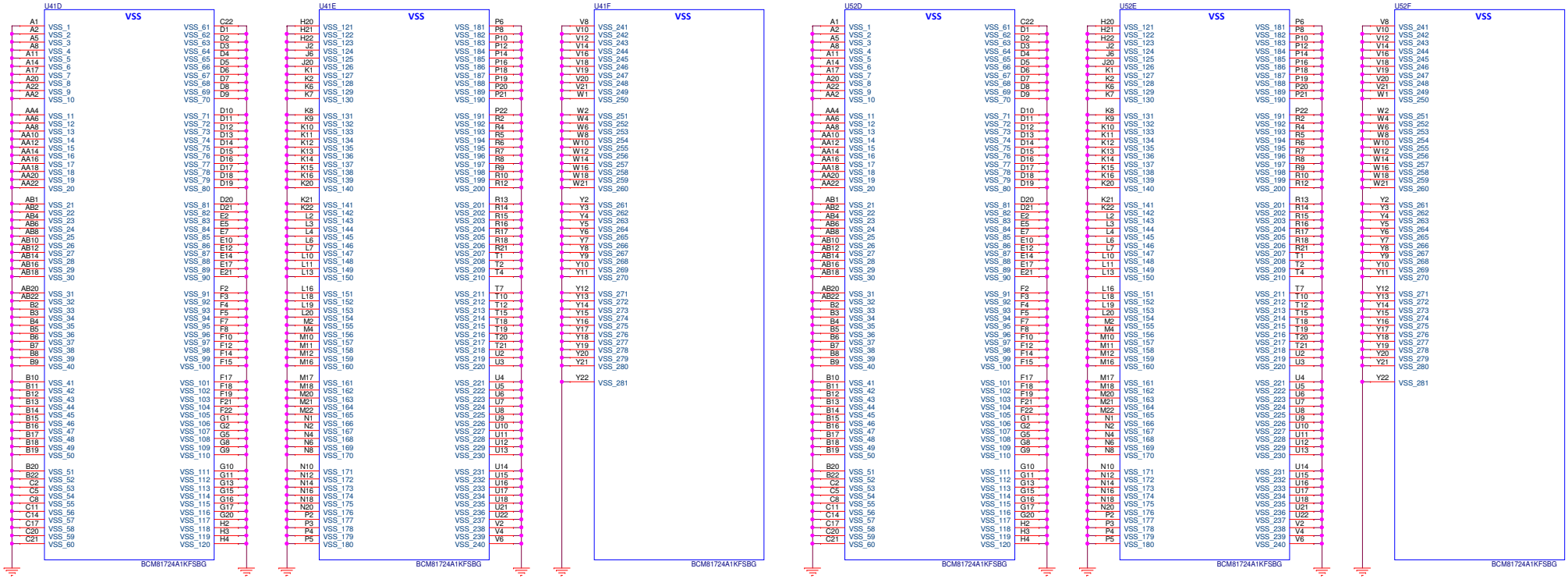
<Core Design>

UfiSpace Co., Ltd.

Title

043_Gearbox GND_01~02

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	43 of 152	015



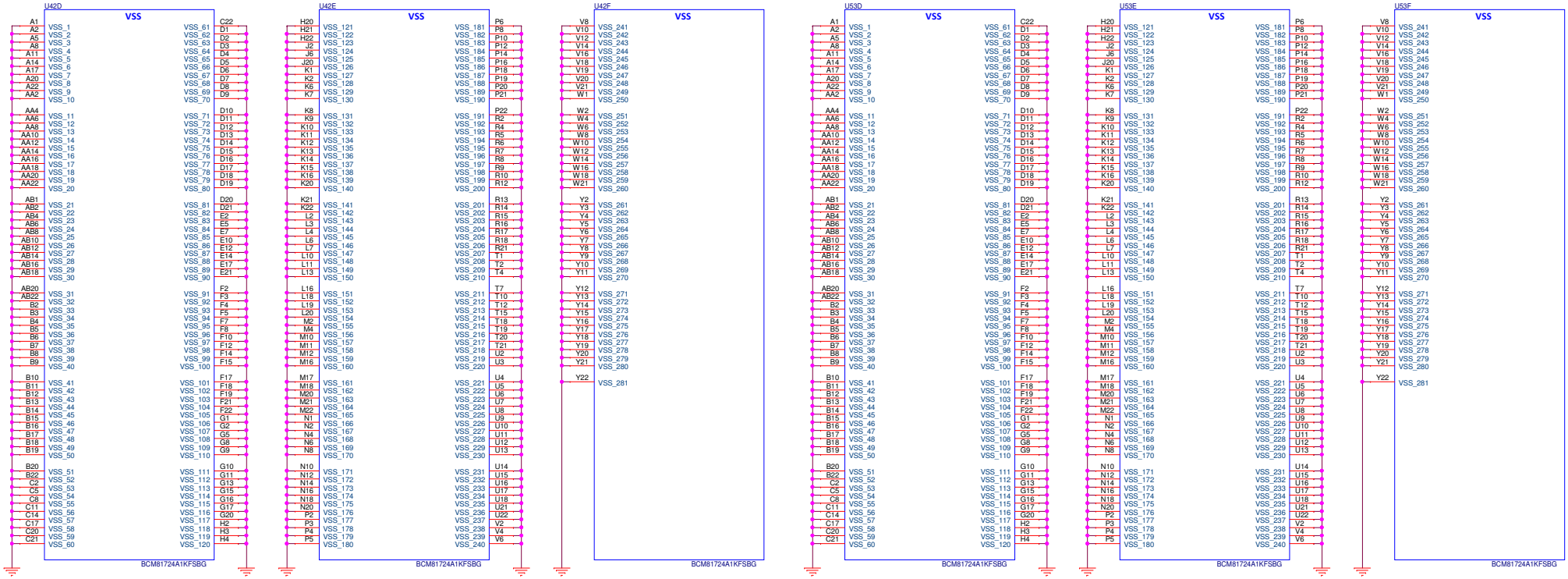
<Core Design>

UfiSpace Co., Ltd.

Title

044_Gearbox GND_03~04

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	44 of 152	015



<Core Design>

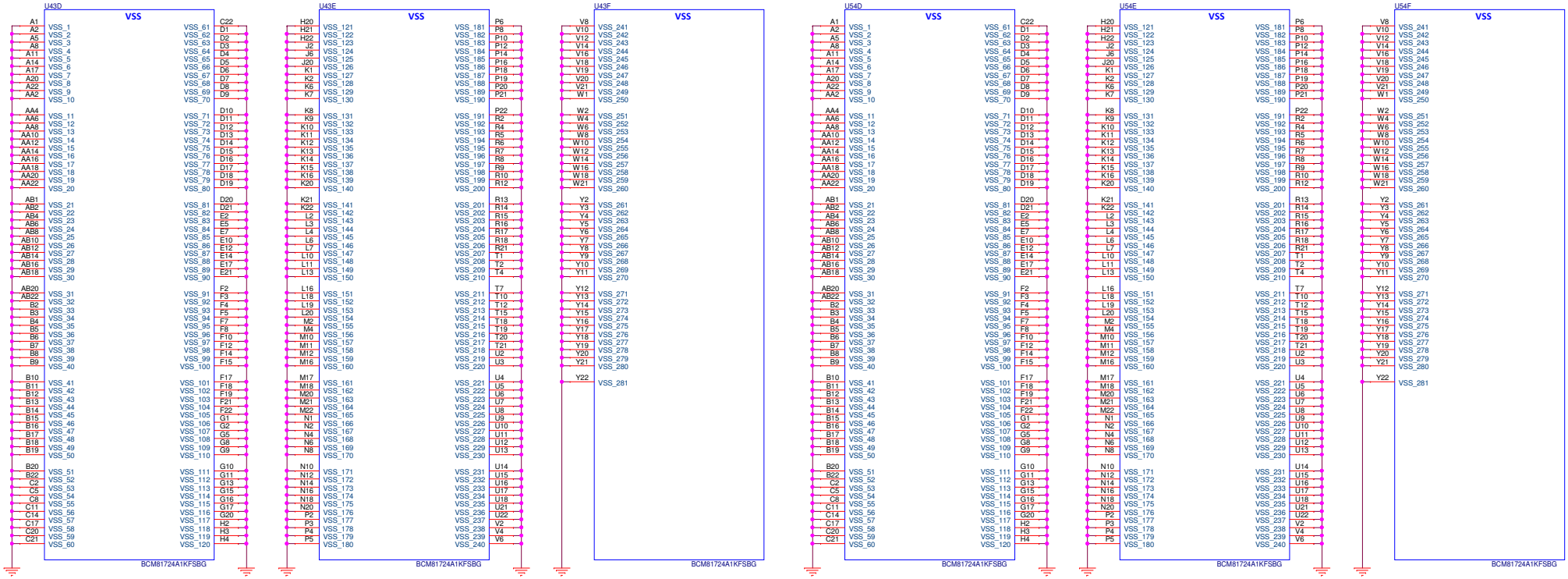
ufiSpace

UfiSpace Co., Ltd.

Title

045_Gearbox GND_05~06

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	45 of 152	015



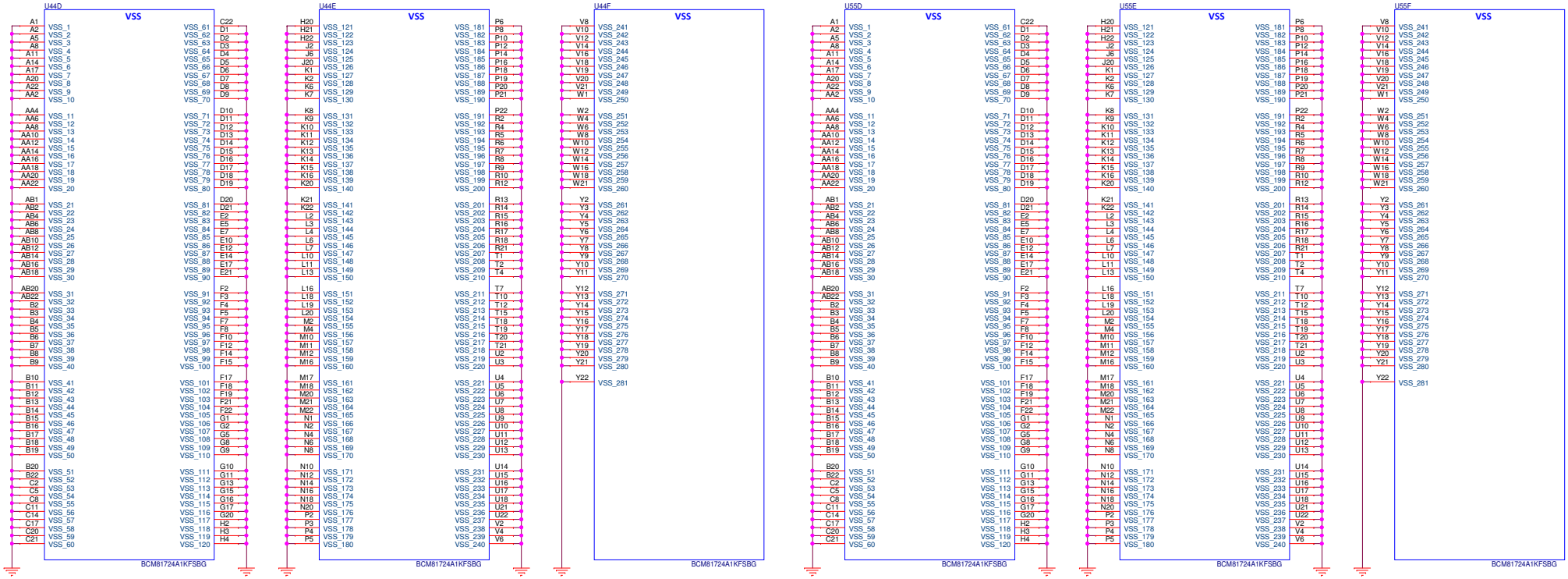
<Core Design>

UfiSpace Co., Ltd.

Title

046_Gearbox GND_07~08

Document Number: PCB P/N: T99O114T00	Sheet 46 of 152	Rev 015



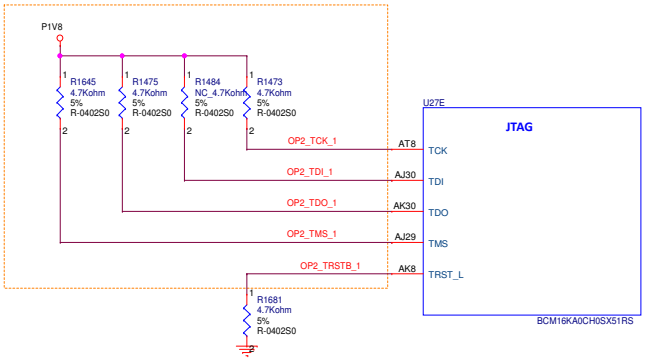
<Core Design>

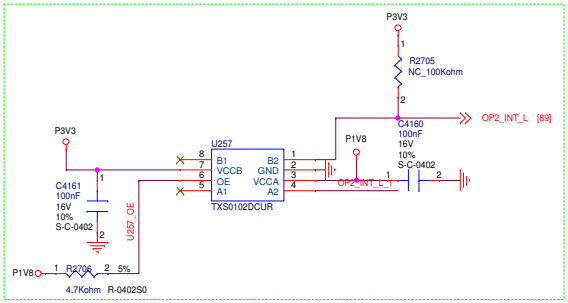
UfiSpace Co., Ltd.

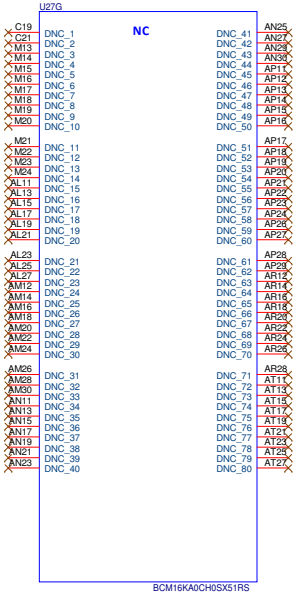
Title

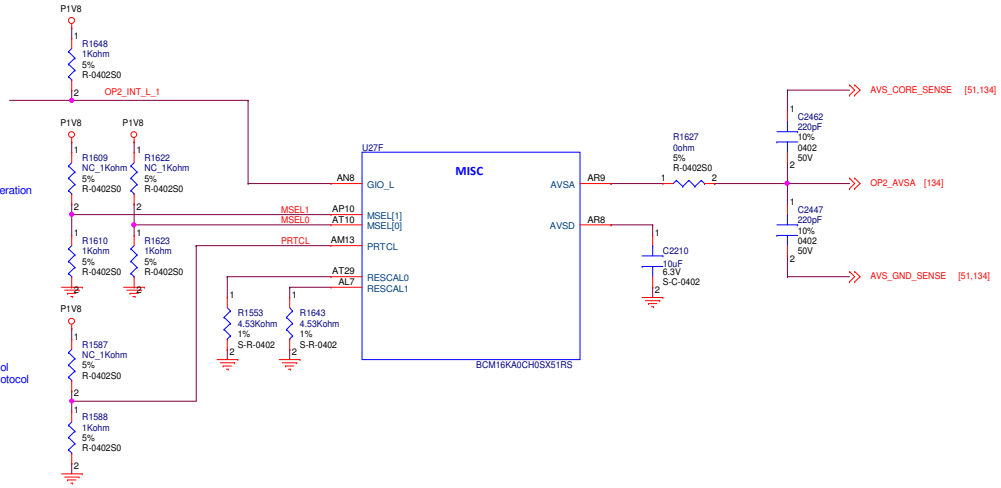
047_Gearbox GND_09~10

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	47 of 152	015





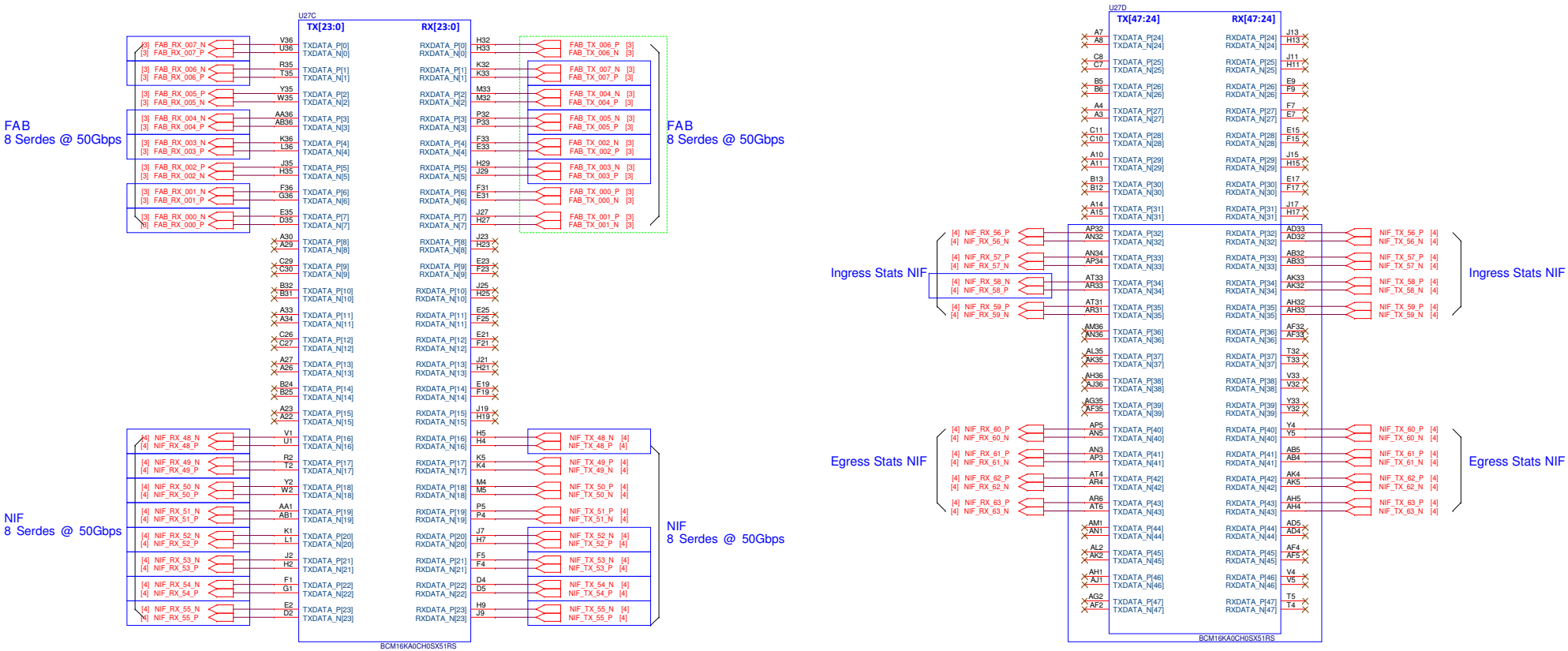




<Core Design>
UfiSpace Co., Ltd.

Title
048_OP2_JTAG_MISC

Document Number:		Sheet	Rev
PCB P/N: T99O114T00		48 of 152	015



<Core Design>

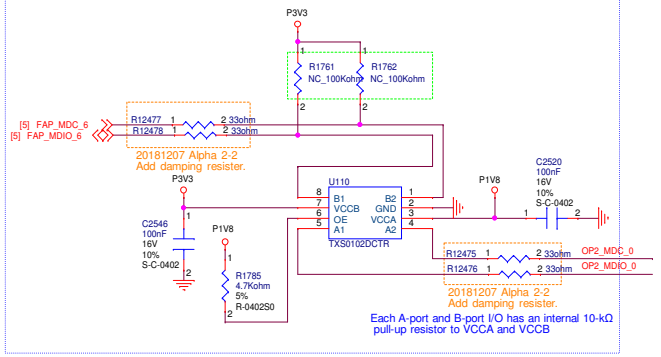
UfiSpace Co., Ltd.

Title

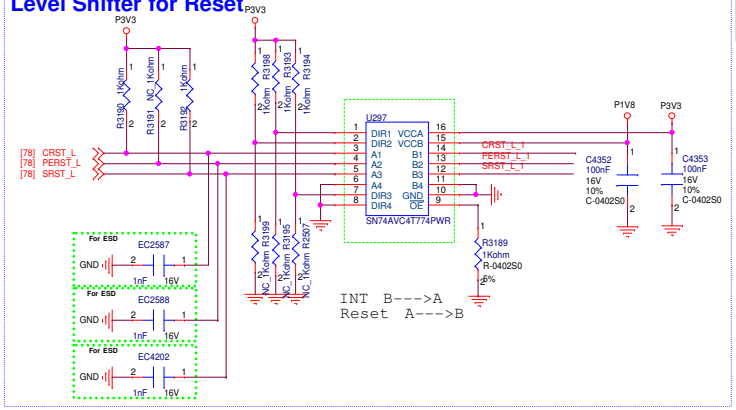
049_OP2_Serdes

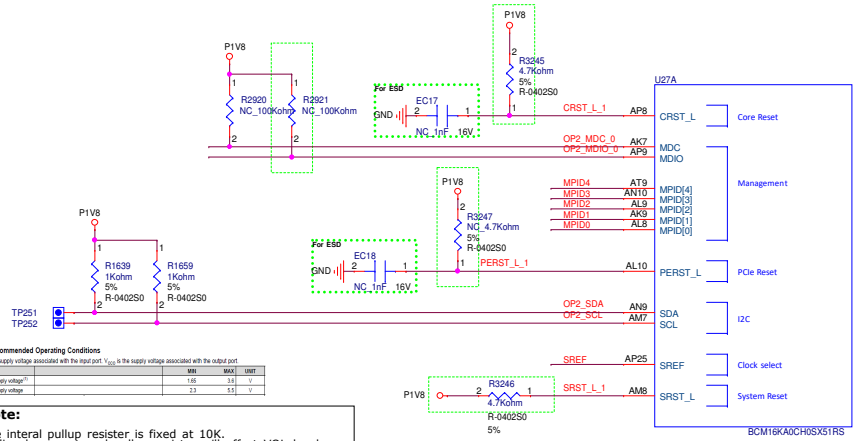
Document Number: PCB P/N: T99O114T00	Sheet 49 of 152	Rev 015

Level Shifter for MDC / MDIO



Level Shifter for Reset





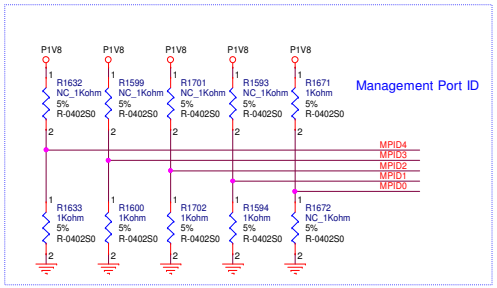
6.3 Recommended Operating Conditions

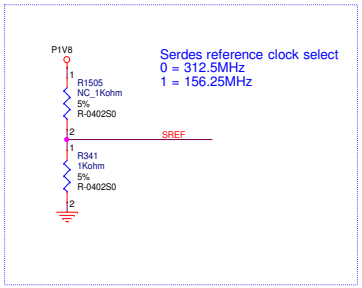
V_{IOA} is the supply voltage associated with the input port. V_{IOB} is the supply voltage associated with the output port.

		MIN	MAX	UNIT
V_{IOA}	Supply voltage[1]	1.65	3.6	V
V_{IOB}	Supply voltage	2.3	5.5	V

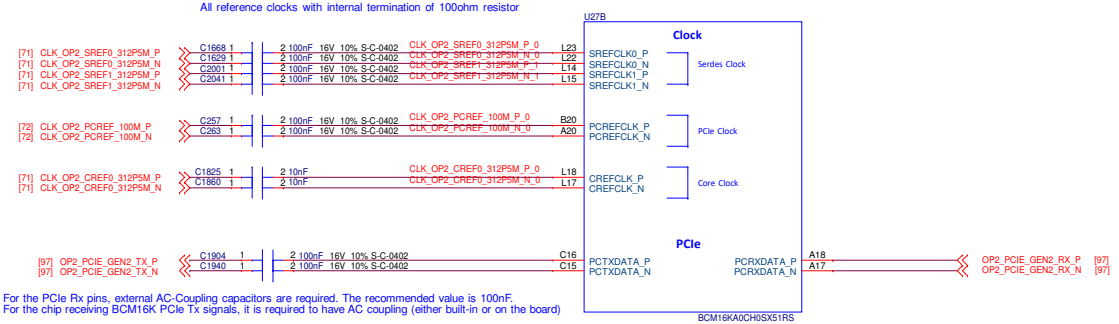
Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.

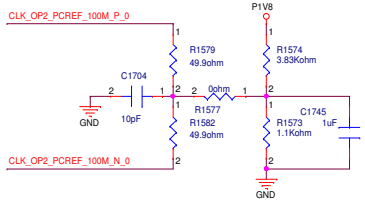




All reference clocks with internal termination of 100ohm resistor



For the PCIe Rx pins, external AC-Coupling capacitors are required. The recommended value is 100nF.
For the chip receiving BCM16K PCIe Tx signals, it is required to have AC coupling (either built-in or on the board)



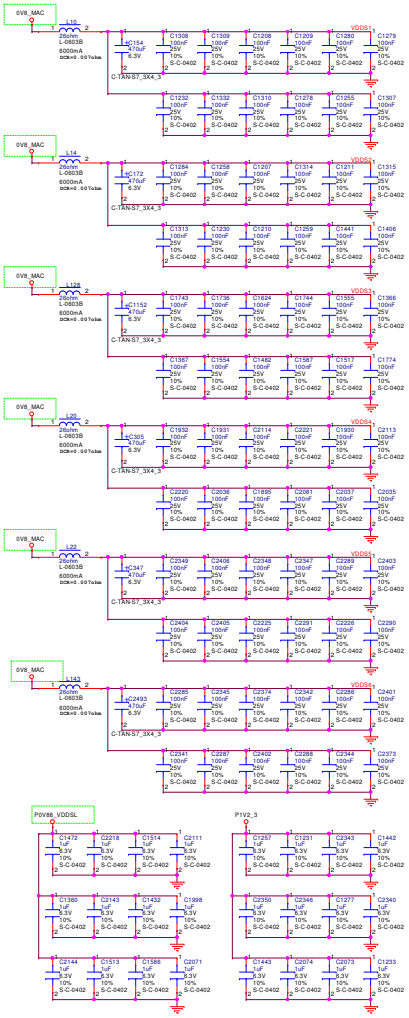
<Core Design>

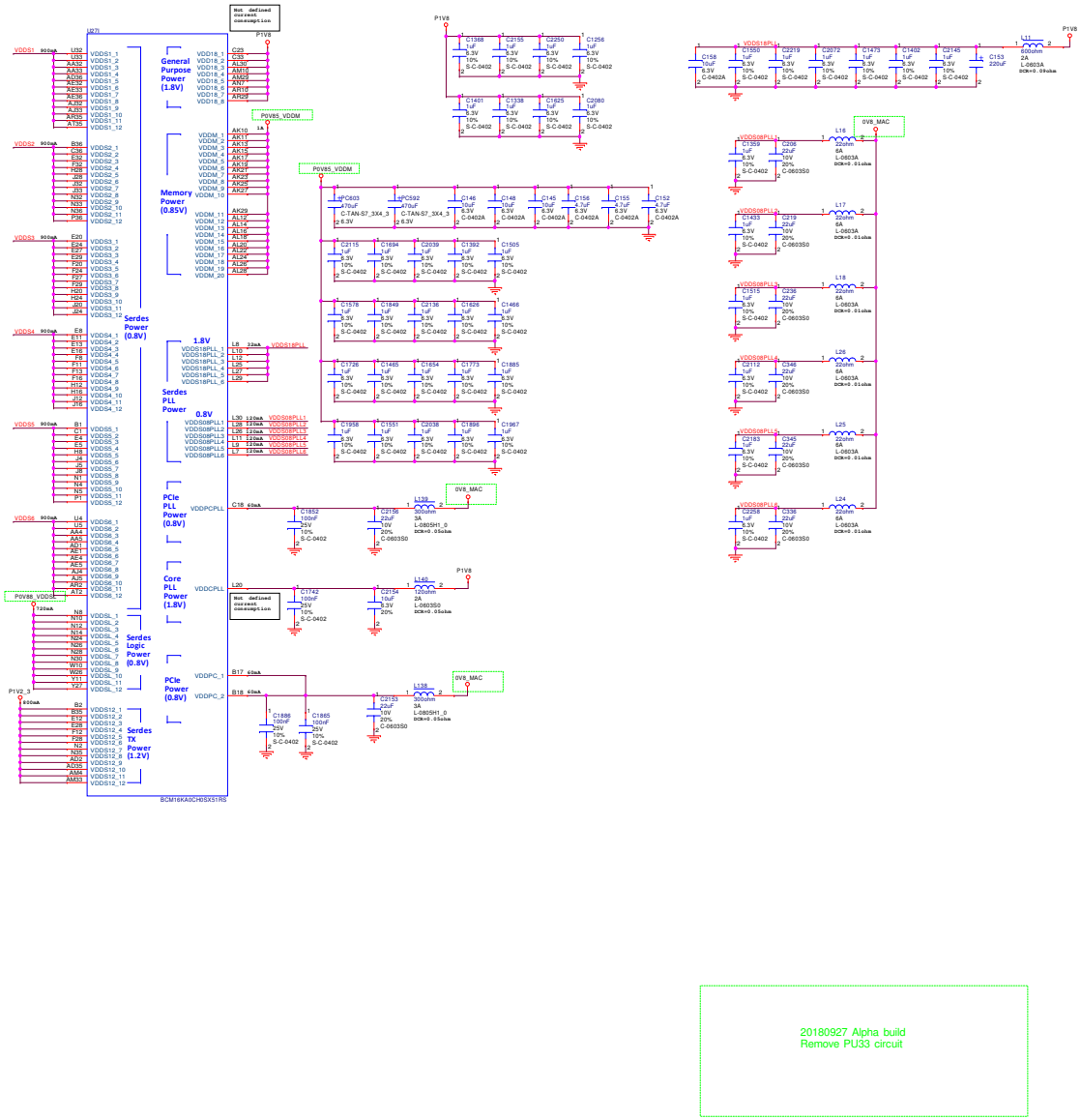
ufiSpace UfiSpace Co., Ltd.

Title: 050_OP2_Reset_Clock_PCIE

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	50 of 152	015


AVS_CORE
U27H
VDD
BCM16KASCHBSX1IRS
4th Position
3rd Position
2nd Position
1st Position
Under BGA
[48,134] AVS_CORE_SENSE
[48,134] AVS_GND_SENSE
TP258
TP254

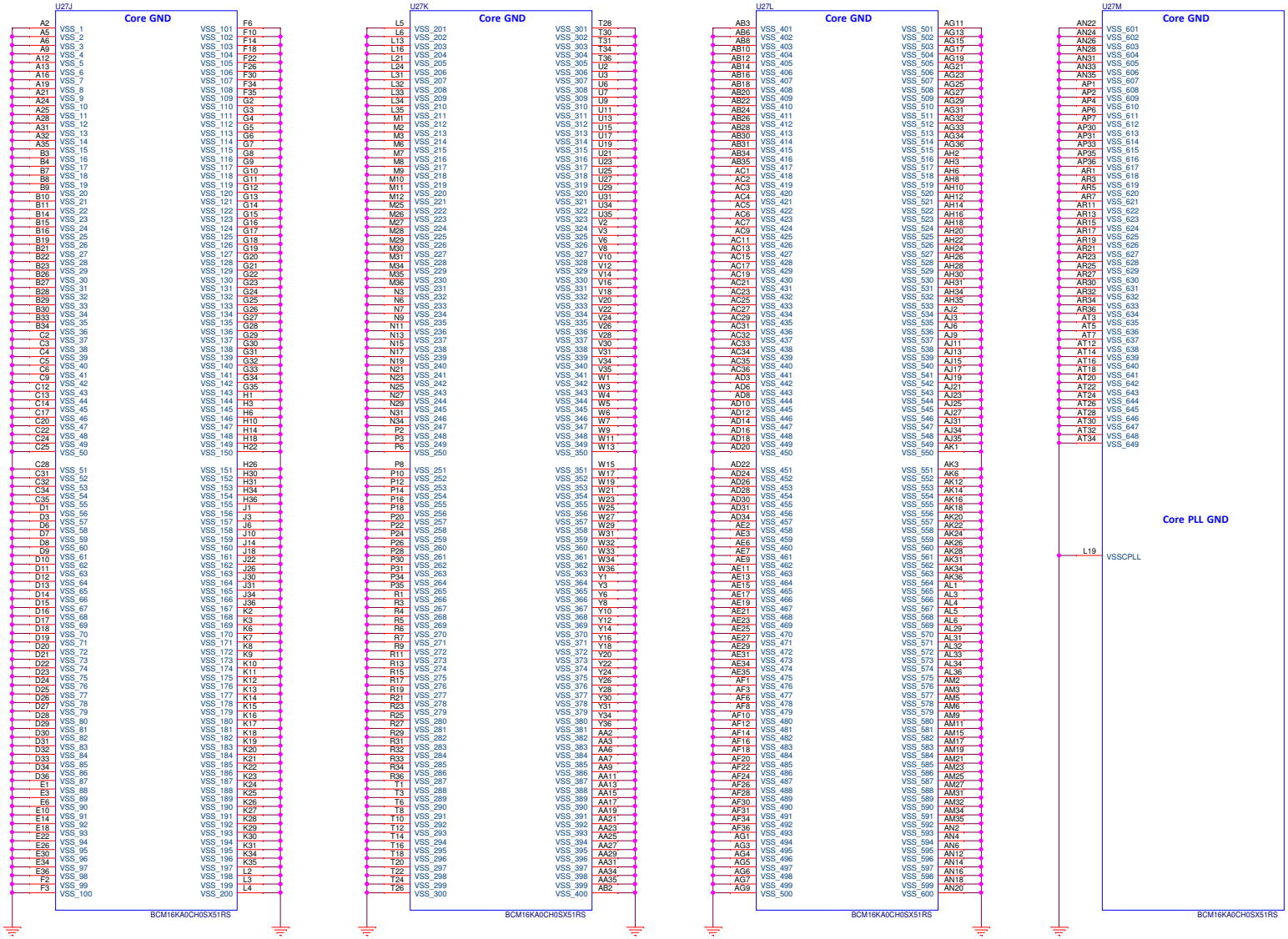




<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title: 052_OP2_Power_VDDM_HVA_LVA_LVD

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	52 of 152	015



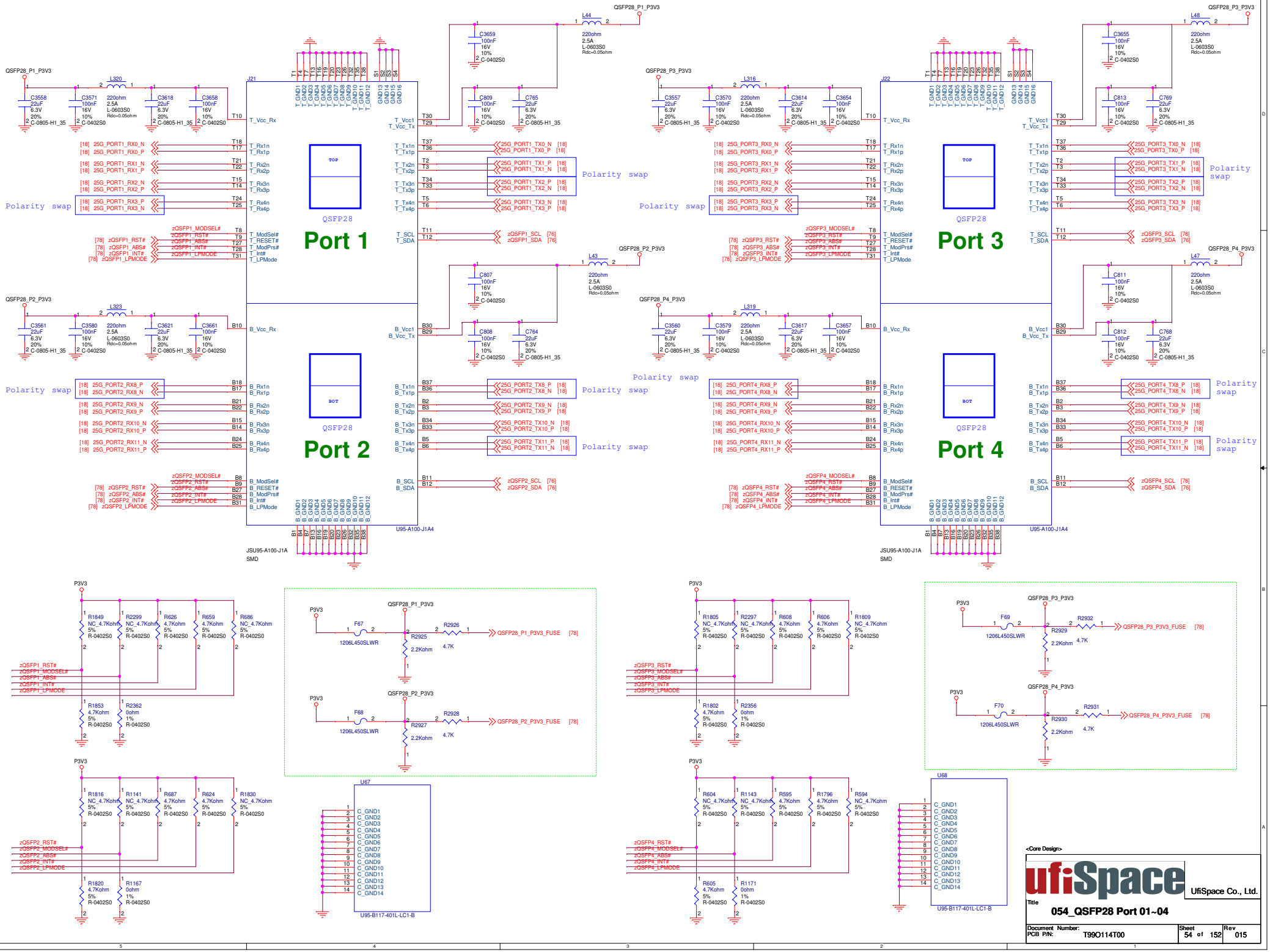
<Core Design>

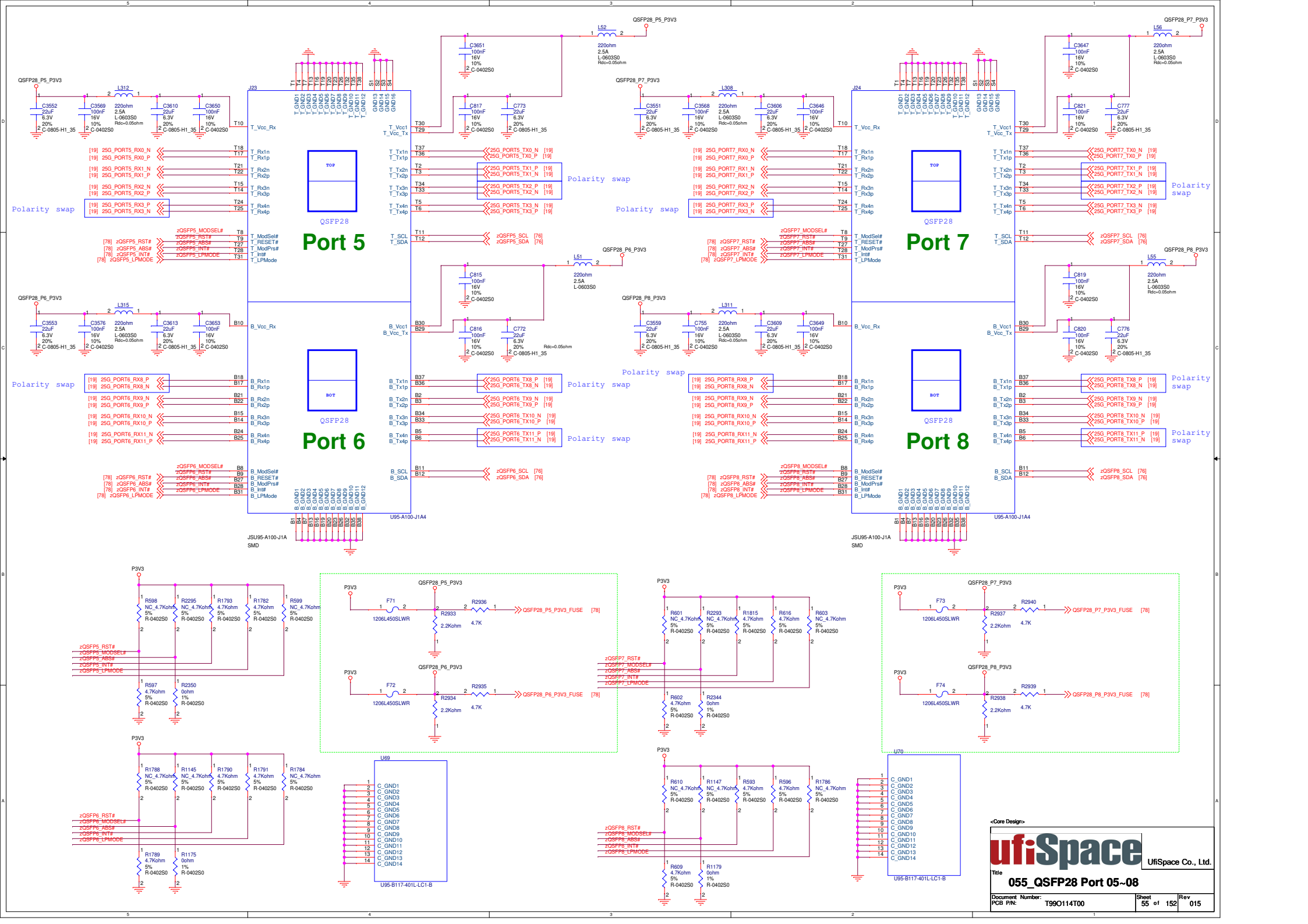
UfiSpace Co., Ltd.

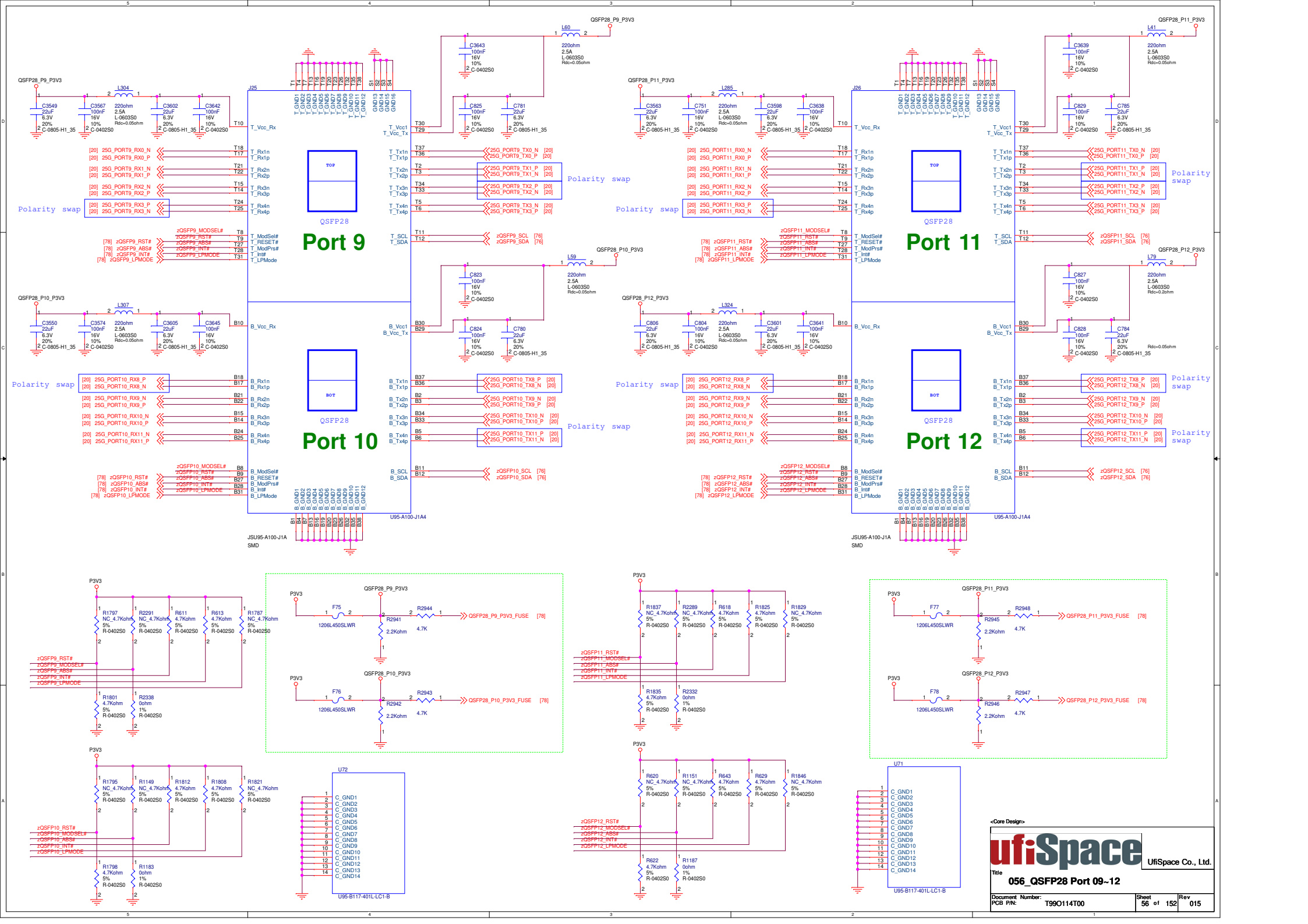
Title

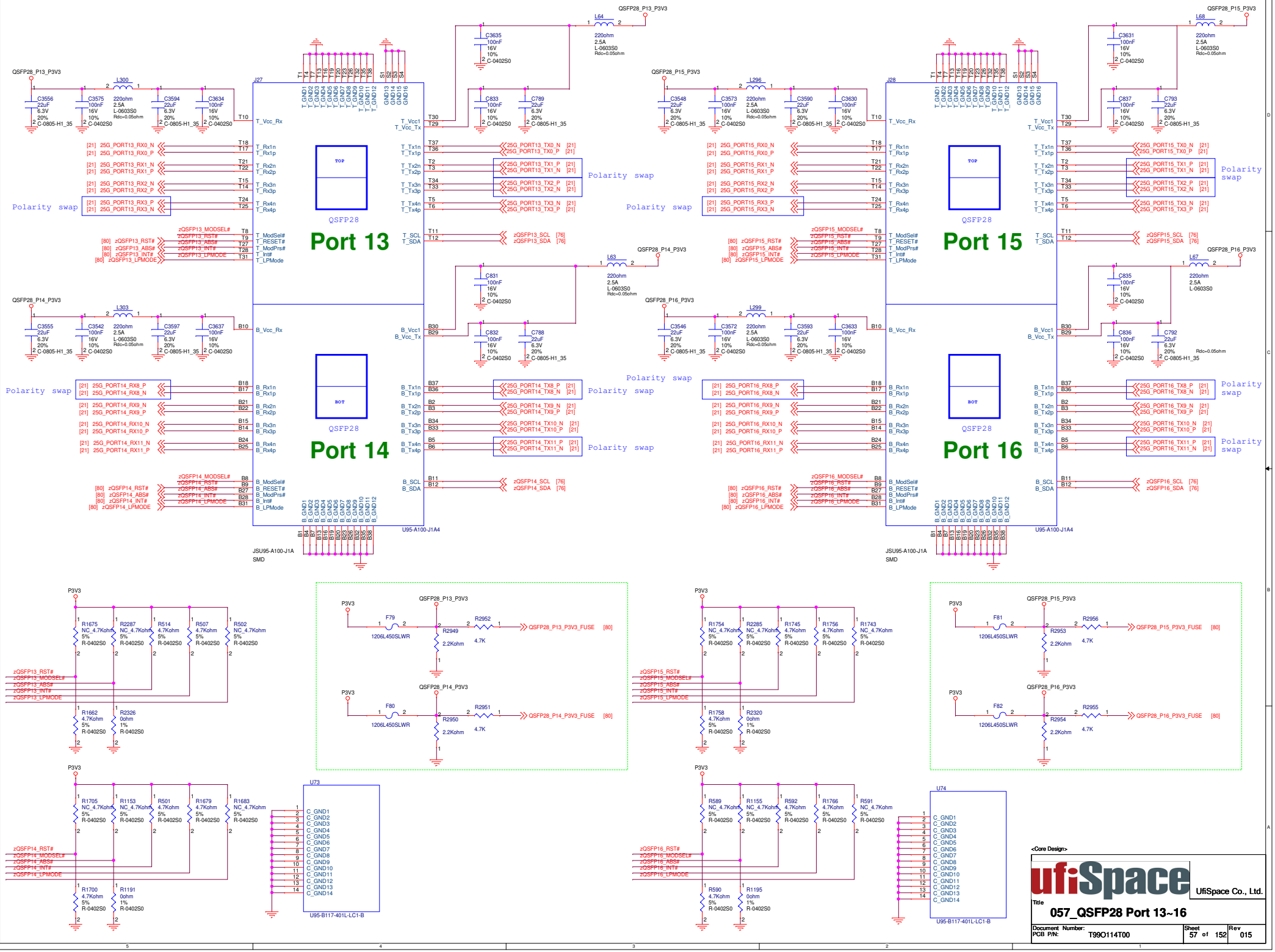
053_OP2_GND

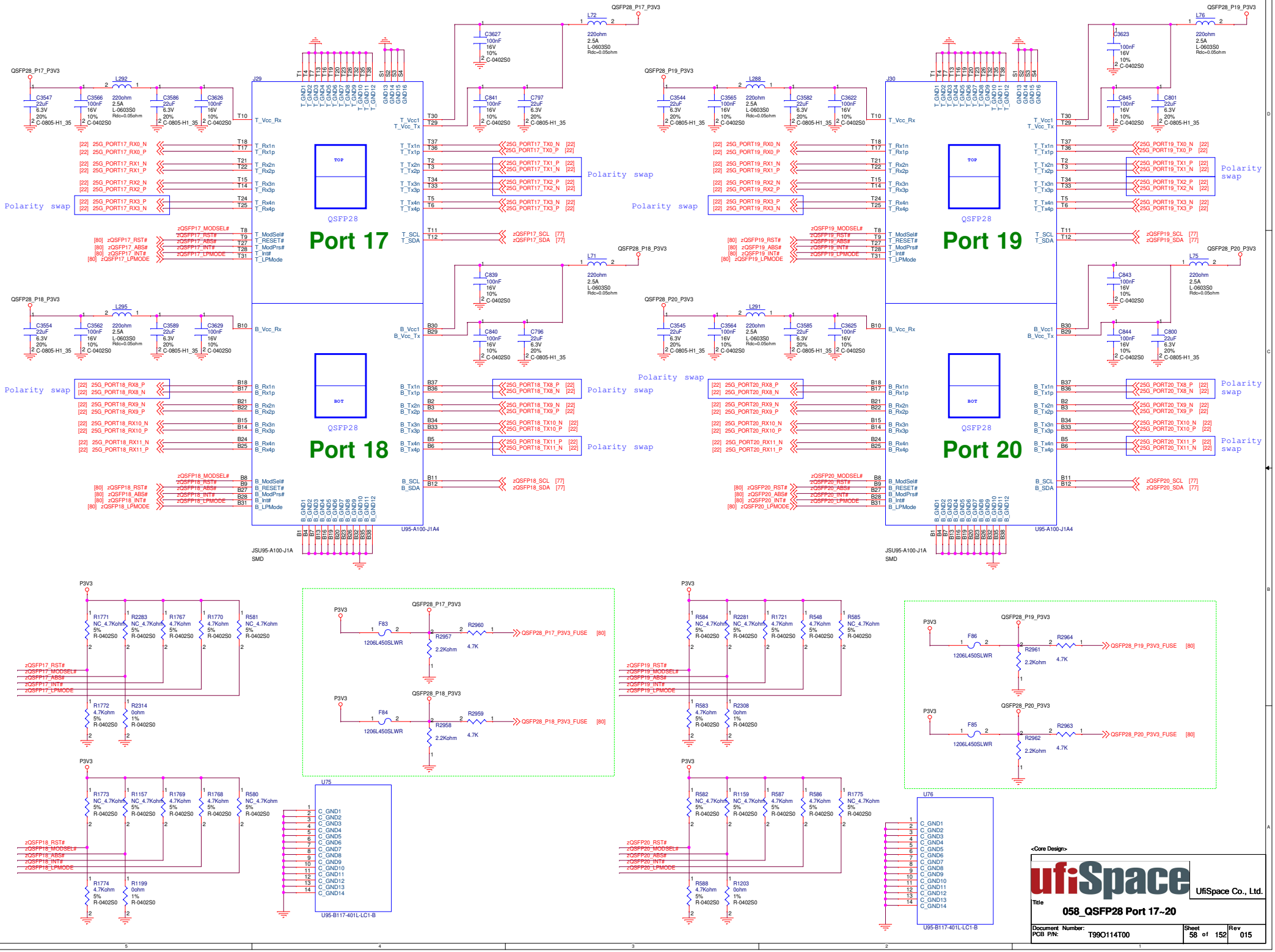
Document Number:		Sheet		Rev
PCB P/N: T99O114T00		53 of 152		015

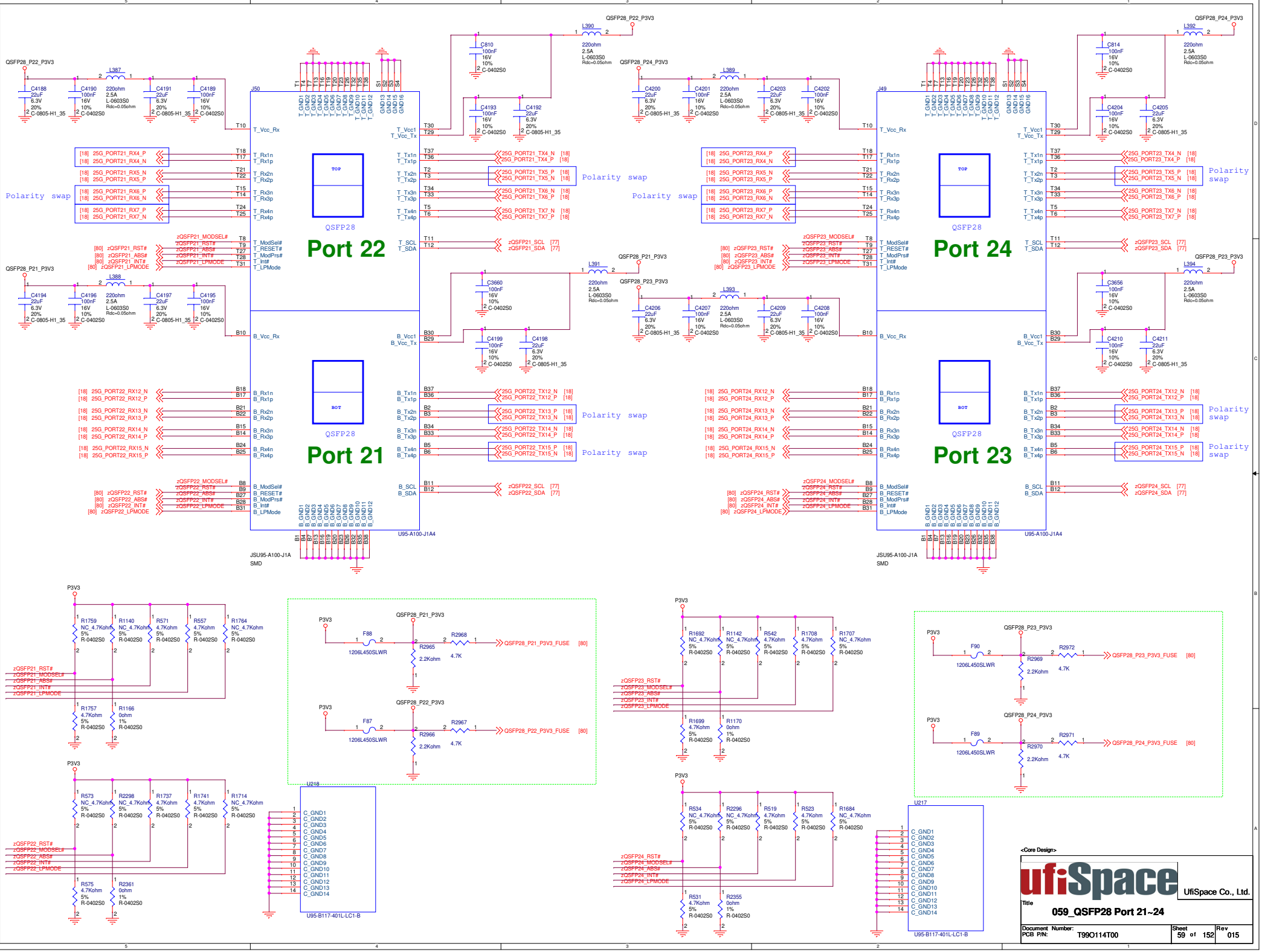

Port 1
Port 2
Port 3
Port 4
QSFP28
TOP
BOT
Polarity swap
J21
J22
U95-A100-J1A4
JSU95-A100-J1A
SMD
U67
U68
U95-B117-401L-LC1-B
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
054_QSFP28 Port 01~04
Document Number:
PCB P/N: T99O114T00
Sheet 54 of 152
Rev 015

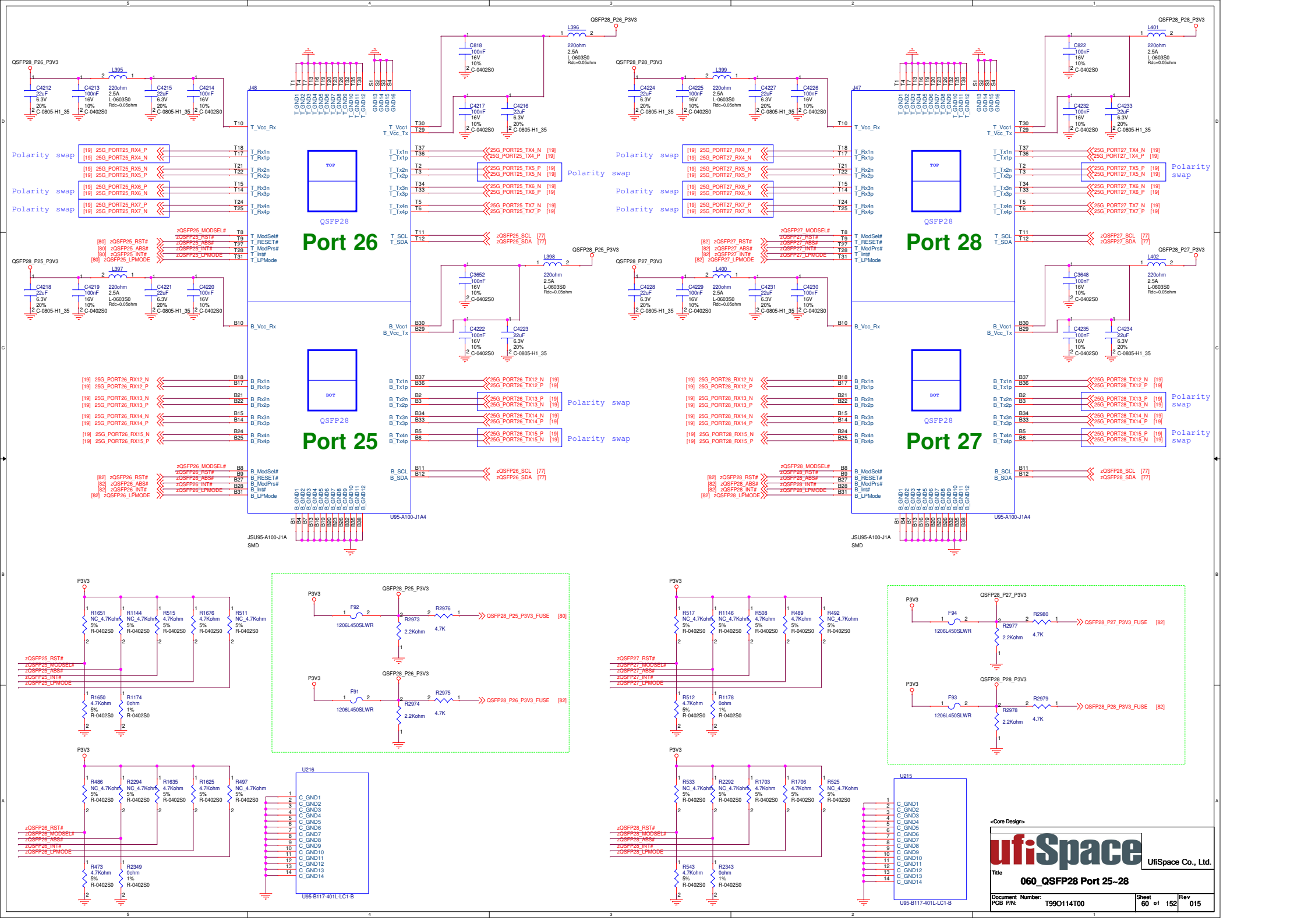

Port 5
Port 6
Port 7
Port 8
QSFP28
Polarity swap
U95-A100-J1A4
JSU95-A100-J1A
SMD
U95-B117-401L-LC1-B
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
055_QSFP28 Port 05~08
Document Number:
PCB P/N: T99O114T00
Sheet 55 of 152
Rev 015

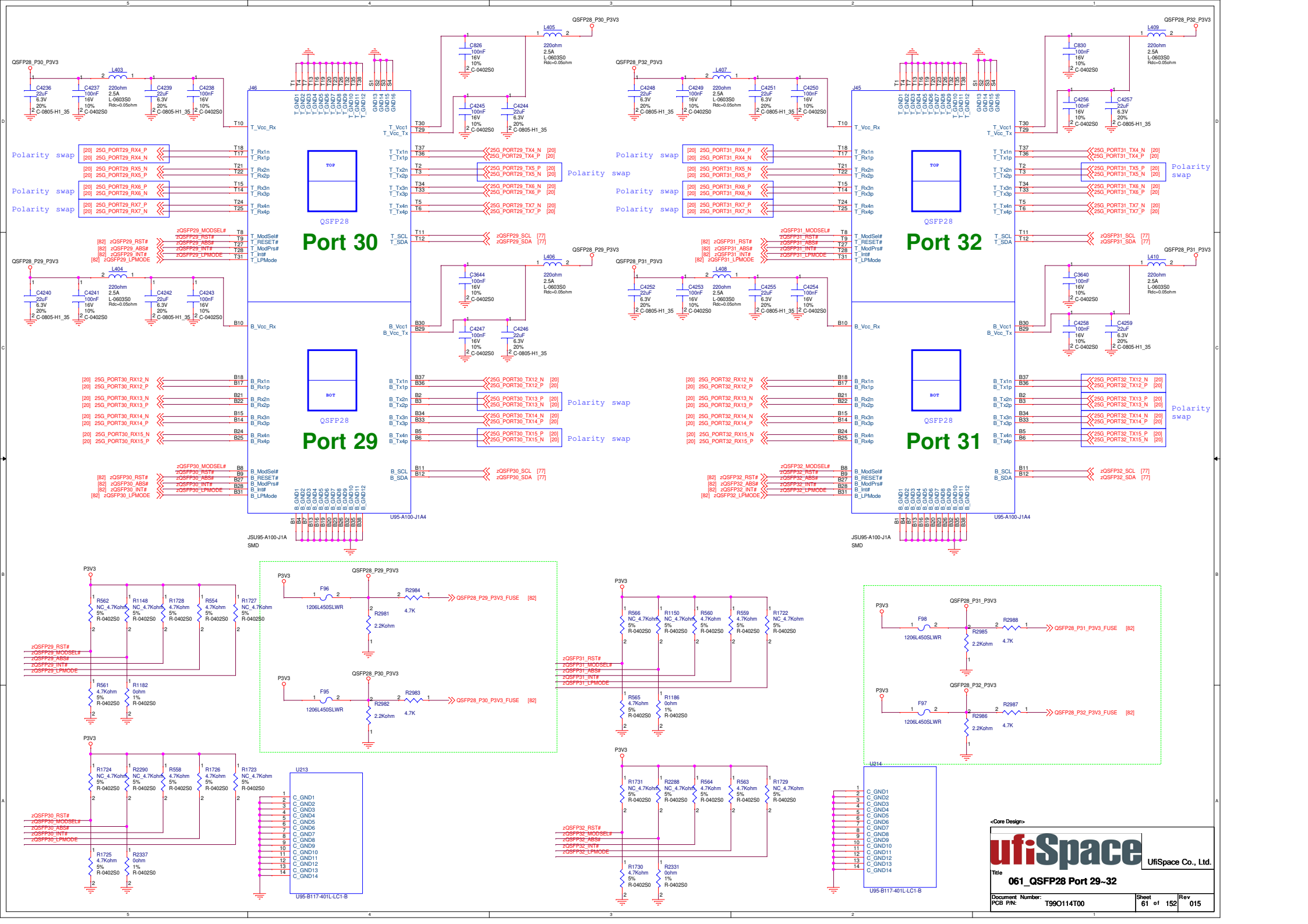

Port 9
Port 10
Port 11
Port 12
QSFP28
Polarity swap
J25
J26
U95-A100-J1A4
JSU95-A100-J1A
SMD
U72
U71
U95-B117-401L-LC1-B
<Core Design>
UfiSpace Co., Ltd.
Title
056_QSFP28 Port 09~12
Document Number:
PCB P/N: T99O114T00
Sheet 56 of 152
Rev 015

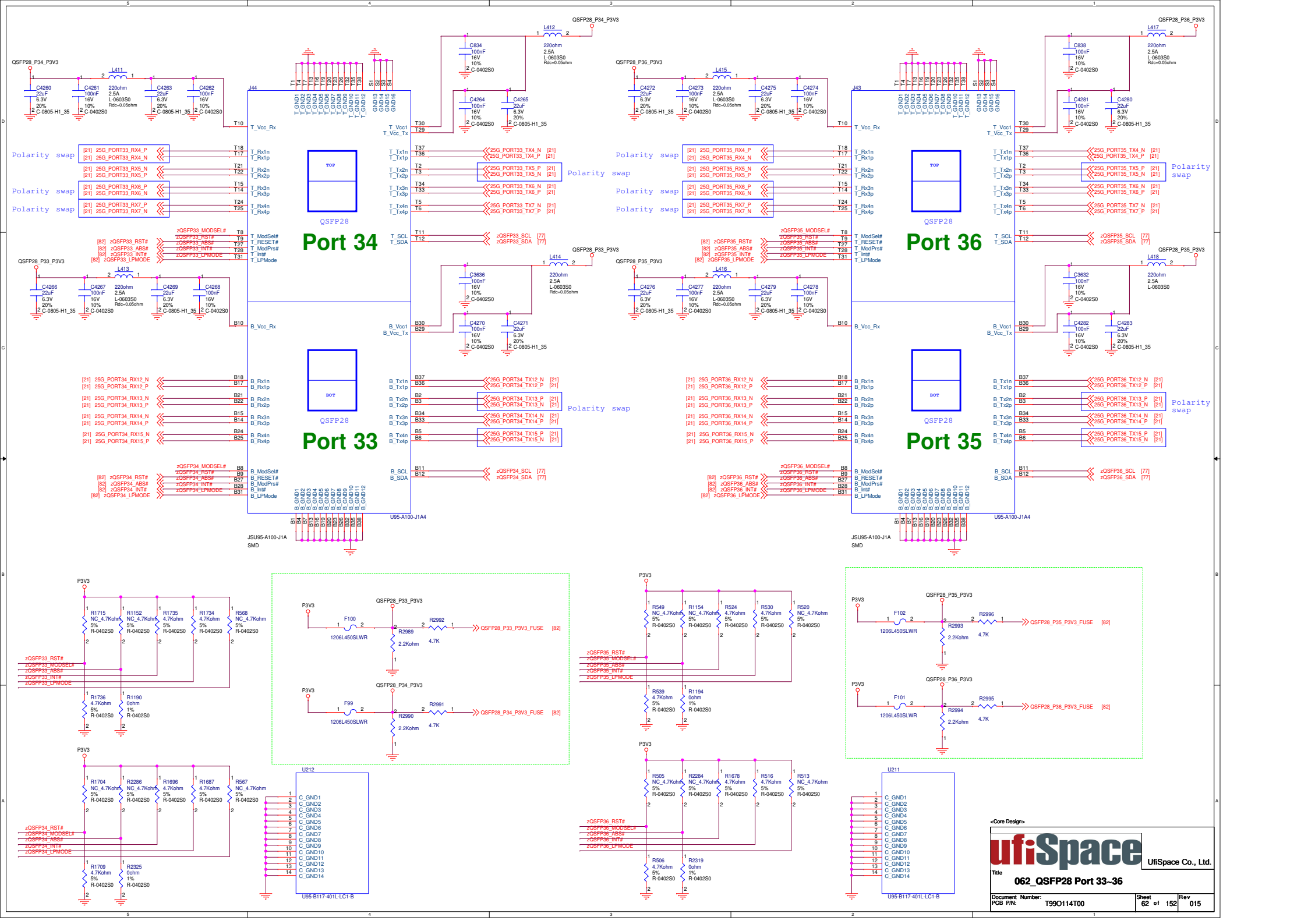

Port 13
Port 14
Port 15
Port 16
QSFP28
Polarity swap
U95-A100-J1A4
JSU95-A100-J1A
SMD
U95-B117-401L-LC1-B
U73
U74
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
057_QSFP28 Port 13~16
Document Number:
PCB P/N: T99O114T00
Sheet 57 of 152
Rev 015

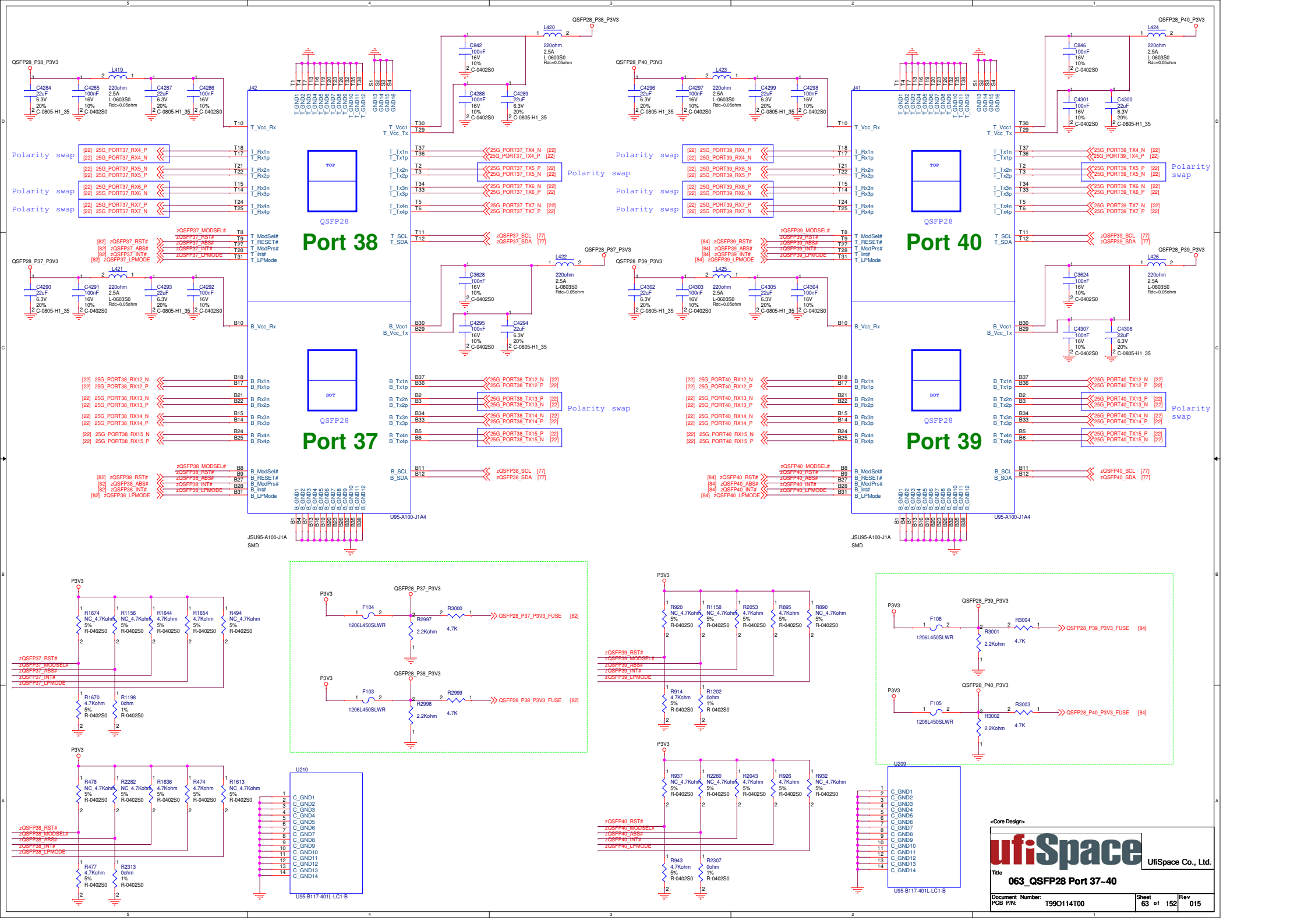

Port 17
Port 18
Port 19
Port 20
QSFP28
TOP
BOT
Polarity swap
U95-A100-J1A4
JSU95-A100-J1A
SMD
U95-B117-401L-LC1-B
U75
U76
1206L450SLWR
220ohm
2.5A
L-0603S0
<Core Design>
UfiSpace Co., Ltd.
Title
058_QSFP28 Port 17~20
Document Number:
PCB P/N: T99O114T00
Sheet 58 of 152
Rev 015


Port 22
Port 21
Port 24
Port 23
QSFP28
TOP
BOT
Polarity swap
J50
J49
JSU95-A100-J1A
SMD
U95-A100-J1A4
U95-B117-401L-LC1-B
U218
U217
QSFP28_P22_P3V3
QSFP28_P21_P3V3
QSFP28_P24_P3V3
QSFP28_P23_P3V3
P3V3
T_Vcc_Rx
T_Vcc1
T_Vcc_Tx
T_Rx1n
T_Rx1p
T_Rx2n
T_Rx2p
T_Rx3n
T_Rx3p
T_Rx4n
T_Rx4p
T_Tx1n
T_Tx1p
T_Tx2n
T_Tx2p
T_Tx3n
T_Tx3p
T_Tx4n
T_Tx4p
T_SCL
T_SDA
T_ModSel#
T_RESET#
T_ModPrs#
T_Int#
T_LPMode
B_Vcc_Rx
B_Vcc1
B_Vcc_Tx
B_Rx1n
B_Rx1p
B_Rx2n
B_Rx2p
B_Rx3n
B_Rx3p
B_Rx4n
B_Rx4p
B_Tx1n
B_Tx1p
B_Tx2n
B_Tx2p
B_Tx3n
B_Tx3p
B_Tx4n
B_Tx4p
B_SCL
B_SDA
B_ModSel#
B_RESET#
B_ModPrs#
B_Int#
B_LPMode
zQSFP21_MODSEL#
zQSFP21_RST#
zQSFP21_ABS#
zQSFP21_INT#
zQSFP21_LPMODE
zQSFP22_MODSEL#
zQSFP22_RST#
zQSFP22_ABS#
zQSFP22_INT#
zQSFP22_LPMODE
zQSFP23_MODSEL#
zQSFP23_RST#
zQSFP23_ABS#
zQSFP23_INT#
zQSFP23_LPMODE
zQSFP24_MODSEL#
zQSFP24_RST#
zQSFP24_ABS#
zQSFP24_INT#
zQSFP24_LPMODE
zQSFP21_SCL [77]
zQSFP21_SDA [77]
zQSFP22_SCL [77]
zQSFP22_SDA [77]
zQSFP23_SCL [77]
zQSFP23_SDA [77]
zQSFP24_SCL [77]
zQSFP24_SDA [77]
C_GND1
C_GND2
C_GND3
C_GND4
C_GND5
C_GND6
C_GND7
C_GND8
C_GND9
C_GND10
C_GND11
C_GND12
C_GND13
C_GND14
QSFP28_P21_P3V3_FUSE [80]
QSFP28_P22_P3V3_FUSE [80]
QSFP28_P23_P3V3_FUSE [80]
QSFP28_P24_P3V3_FUSE [80]
1206L450SLWR
F88
F87
F90
F89
R2965
R2966
R2969
R2970
2.2Kohm
R2968
R2967
R2972
R2971
4.7K
L387
L388
L389
L390
L391
L392
L393
L394
220ohm
2.5A
L-0603S0
Rdc=0.05ohm
C4188
C4189
C4190
C4191
C4194
C4195
C4196
C4197
C4200
C4201
C4202
C4203
C4206
C4207
C4208
C4209
22uF
6.3V
20%
C-0805-H1_35
100nF
16V
10%
C-0402S0
C810
C4193
C4192
C3660
C4199
C4198
C814
C4204
C4205
C3656
C4210
C4211
R1759
R1140
R571
R557
R1764
R1757
R1166
R573
R2298
R1737
R1741
R1714
R575
R2361
R1692
R1142
R542
R1708
R1707
R1699
R1170
R534
R2296
R519
R523
R1684
R531
R2355
NC_4.7Kohm
4.7Kohm
0ohm
5%
1%
R-0402S0
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
059_QSFP28 Port 21~24
Document Number:
PCB P/N:
T99O114T00
Sheet
59 of 152
Rev
015


Port 26
Port 25
Port 28
Port 27
QSFP28
J48
J47
U95-A100-J1A4
JSU95-A100-J1A
SMD
U216
U215
U95-B117-401L-LC1-B
Polarity swap
<Core Design>
UfiSpace Co., Ltd.
Title
060_QSFP28 Port 25~28
Document Number:
PCB P/N: T99O114T00
Sheet 60 of 152
Rev 015


Port 30
Port 29
Port 32
Port 31
QSFP28
Polarity swap
J46
J45
U95-A100-J1A4
JSU95-A100-J1A
SMD
U213
U214
U95-B117-401L-LC1-B
1206L450SLWR
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
061_QSFP28 Port 29~32
Document Number:
PCB P/N: T99O114T00
Sheet 61 of 152
Rev 015


Port 34
Port 33
Port 36
Port 35
QSFP28
TOP
BOT
Polarity swap
U95-A100-J1A4
JSU95-A100-J1A
SMD
U95-B117-401L-LC1-B
U212
U211
F100
F99
F102
F101
1206L450SLWR
<Core Design>
UfiSpace Co., Ltd.
062_QSFP28 Port 33~36
Document Number:
PCB P/N: T99O114T00
Sheet 62 of 152
Rev 015


Port 38
Port 37
Port 40
Port 39
QSFP28
TOP
BOT
Polarity swap
J42
J41
U95-A100-J1A4
JSU95-A100-J1A
SMD
U210
U209
U95-B117-401L-LC1-B
P3V3
QSFP28_P38_P3V3
QSFP28_P37_P3V3
QSFP28_P40_P3V3
QSFP28_P39_P3V3
QSFP28_P37_P3V3_FUSE [82]
QSFP28_P38_P3V3_FUSE [82]
QSFP28_P39_P3V3_FUSE [84]
QSFP28_P40_P3V3_FUSE [84]
1206L450SLWR
F104
F103
F106
F105
R3000
R2999
R3004
R3003
R2997
R2998
R3001
R3002
2.2Kohm
4.7K
<Core Design>
UfiSpace Co., Ltd.
Title
063_QSFP28 Port 37~40
Document Number:
PCB P/N: T99O114T00
Sheet 63 of 152
Rev 015

2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

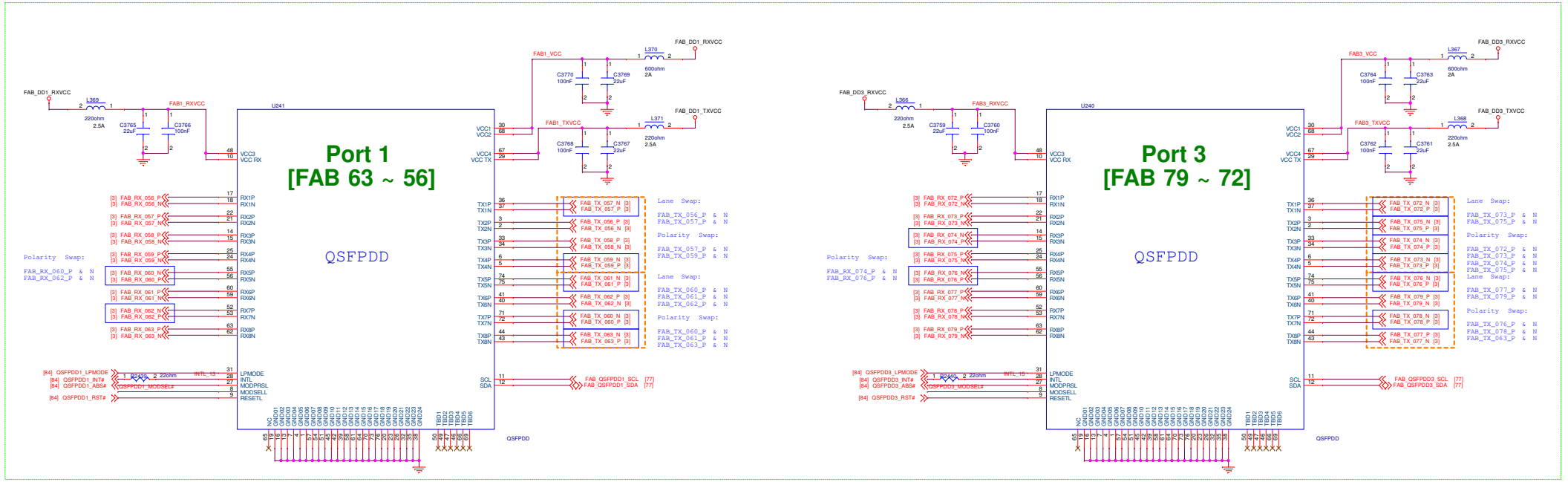
2.4.1 Blackhawk Lane Mapping – Fabric

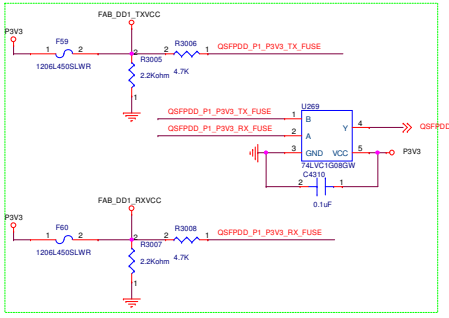
Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

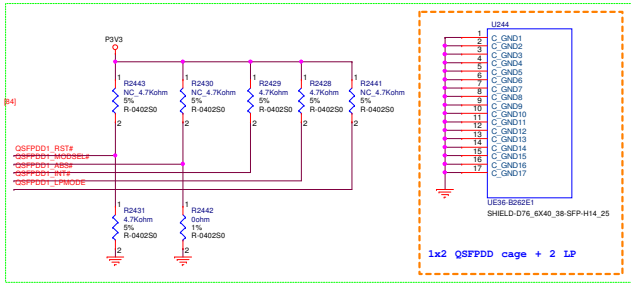
The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

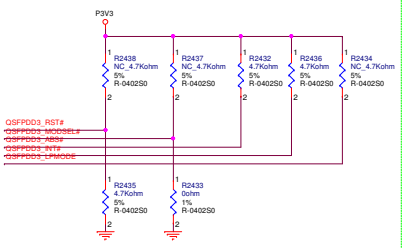
FAB Port Mapping

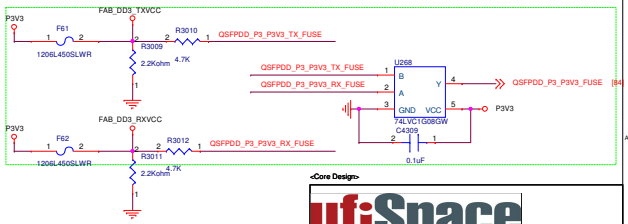
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	











2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

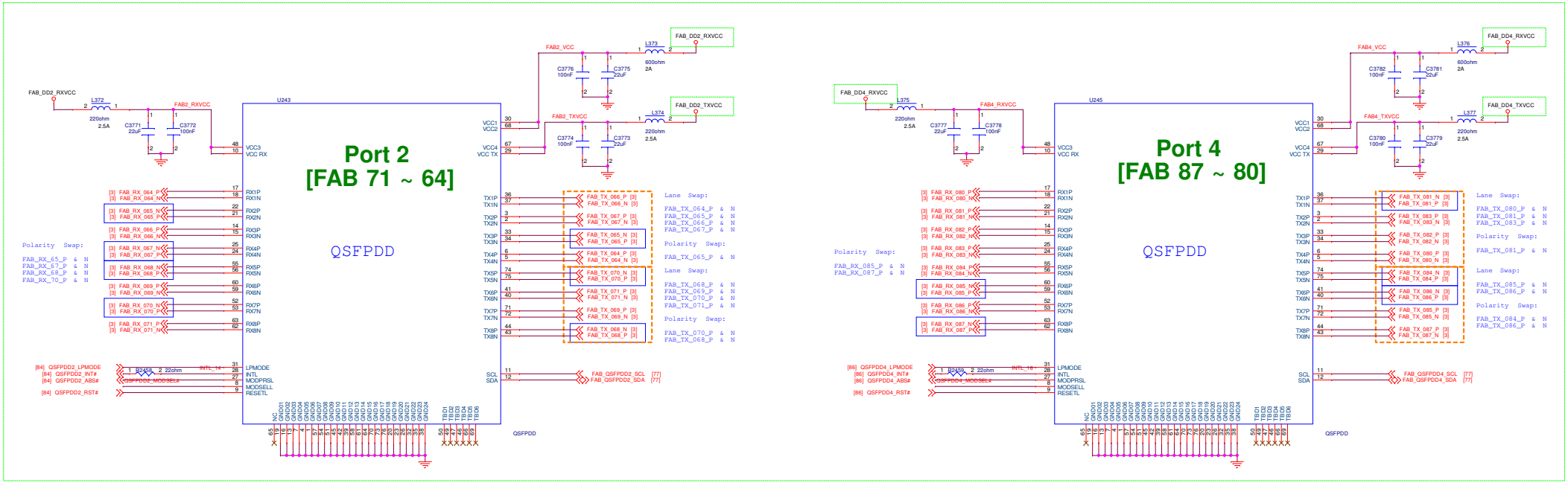
2.4.1 Blackhawk Lane Mapping – Fabric

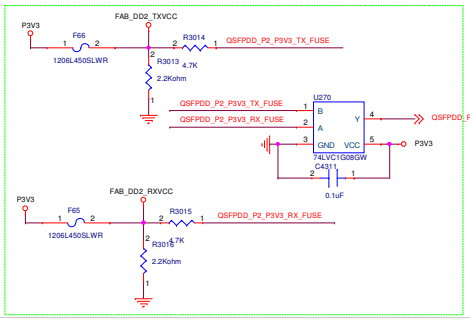
Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

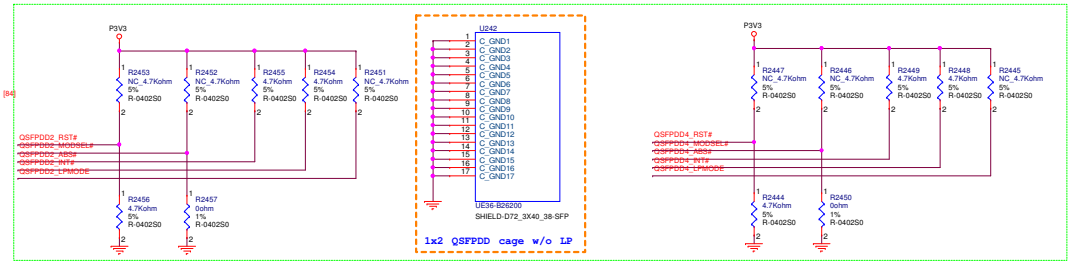
The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

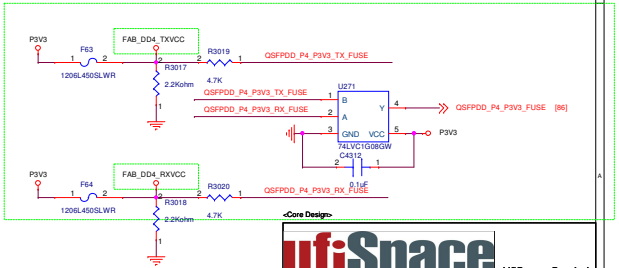
FAB Port Mapping

Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	









ufiSpace UfiSpace Co., Ltd.

Title: 065_QSFPDD3~4

Document Number: T99O114T00 | Sheet 65 of 152 | Rev 015

2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

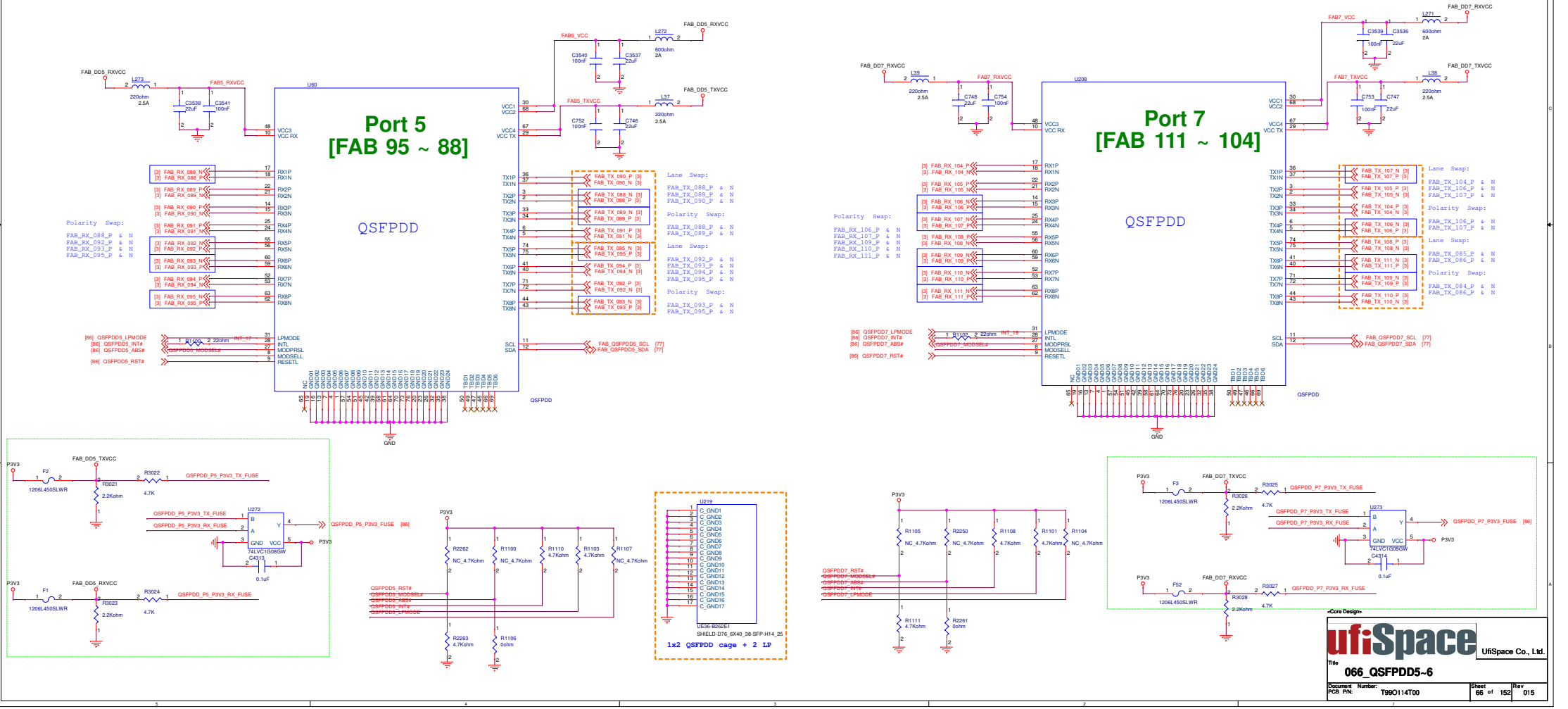
2.4.1 Blackhawk Lane Mapping – Fabric

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

FAB Port Mapping

Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	



Confidential

2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

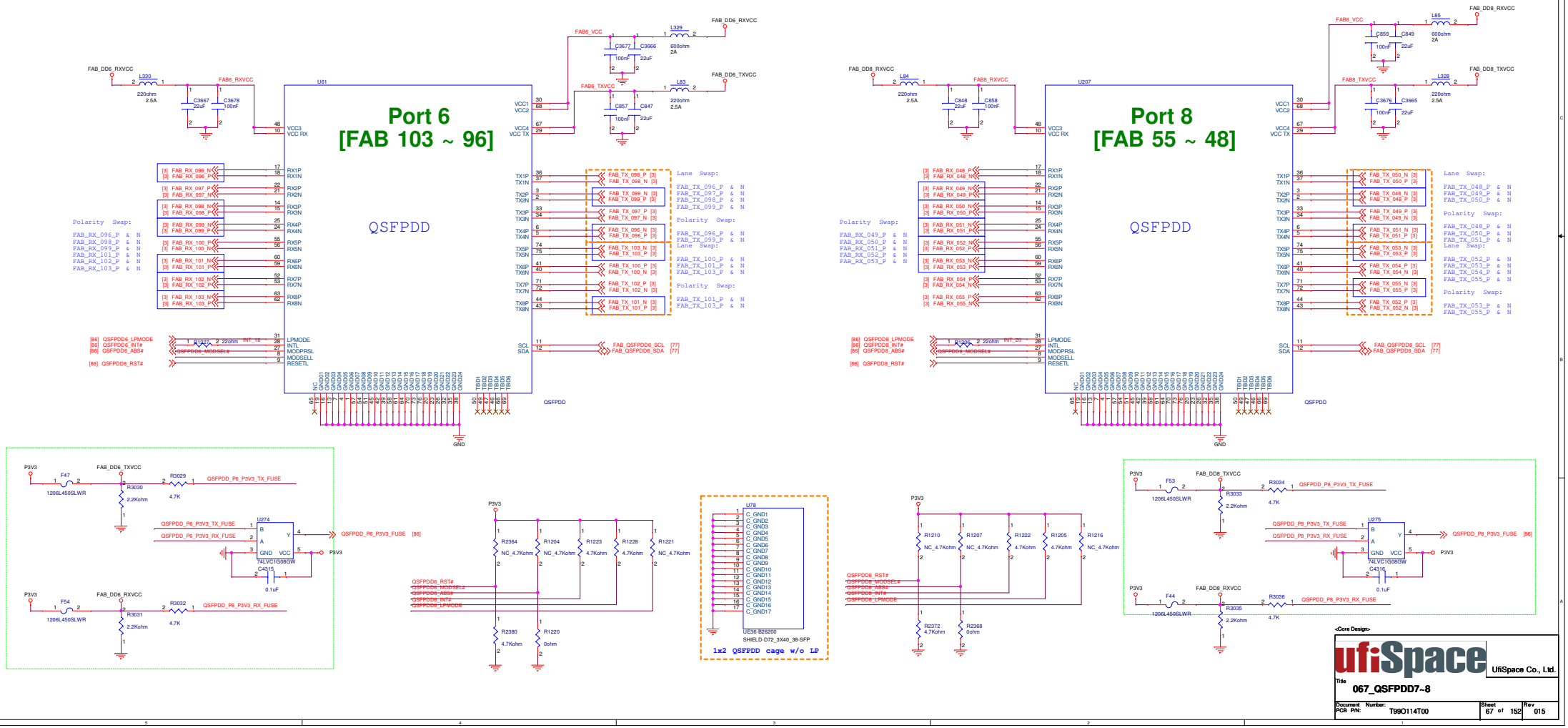
2.4.1 Blackhawk Lane Mapping – Fabric

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

FAB Port Mapping

Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	



2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

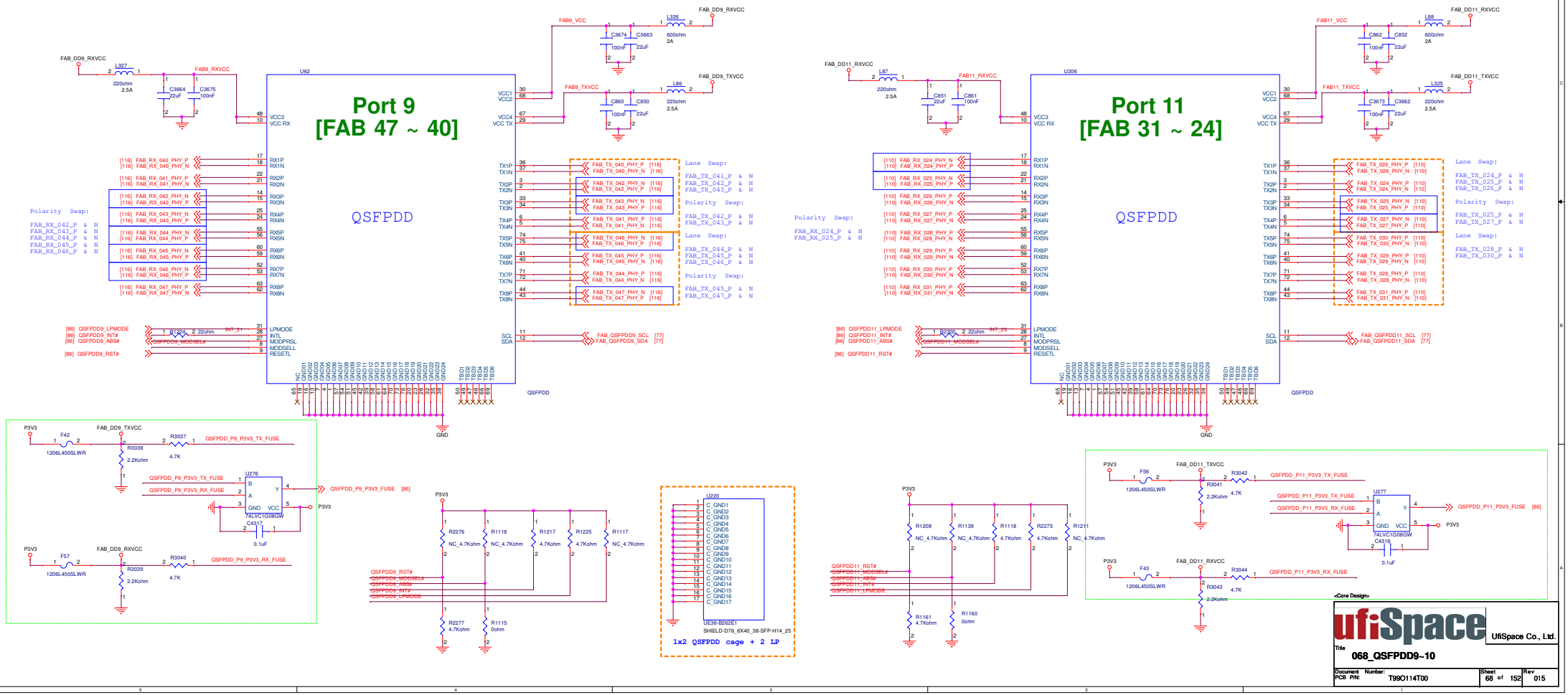
2.4.1 Blackhawk Lane Mapping – Fabric

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

FAB Port Mapping

Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	



2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

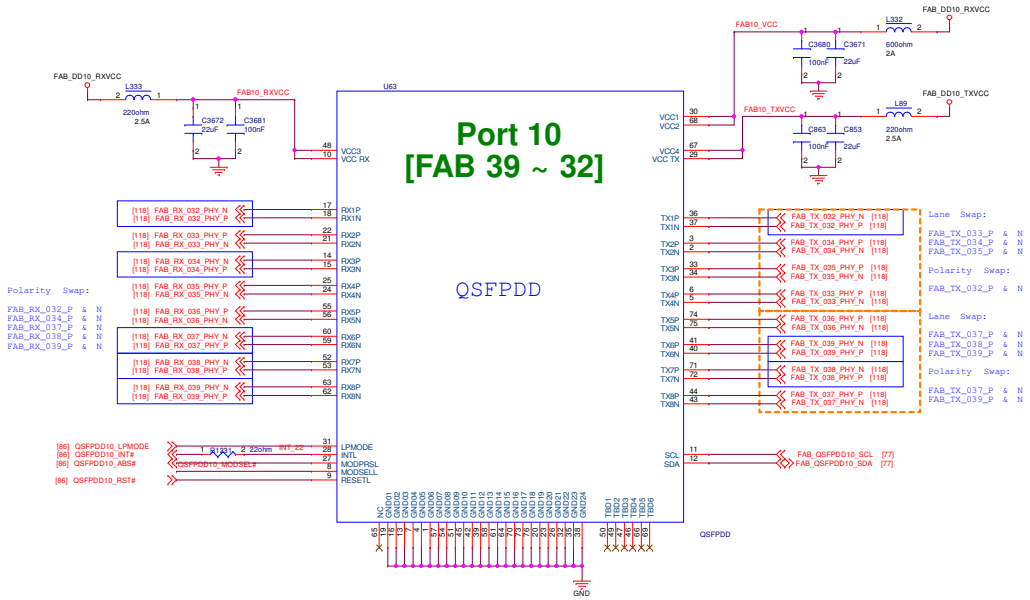
2.4.1 Blackhawk Lane Mapping – Fabric

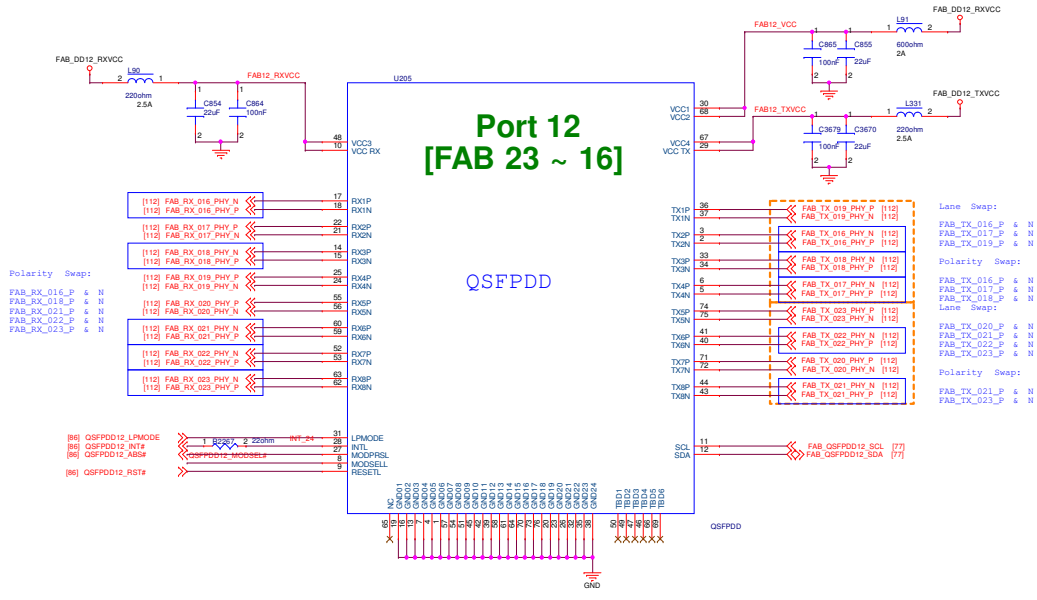
Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

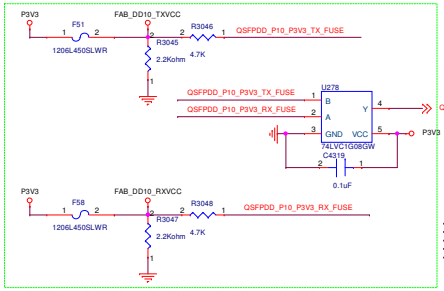
The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

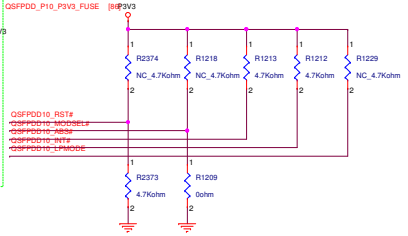
FAB Port Mapping

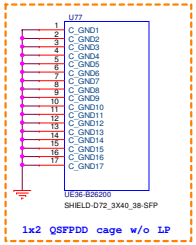
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	

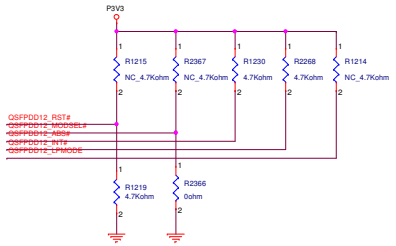


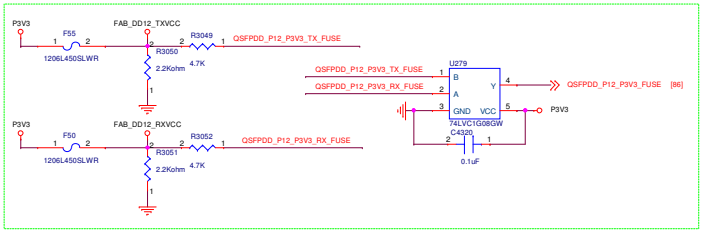












<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
069_QSFPDD11~12
Document Number:
PCB P/N: T99O114T00
Sheet 69 of 152
Rev 015

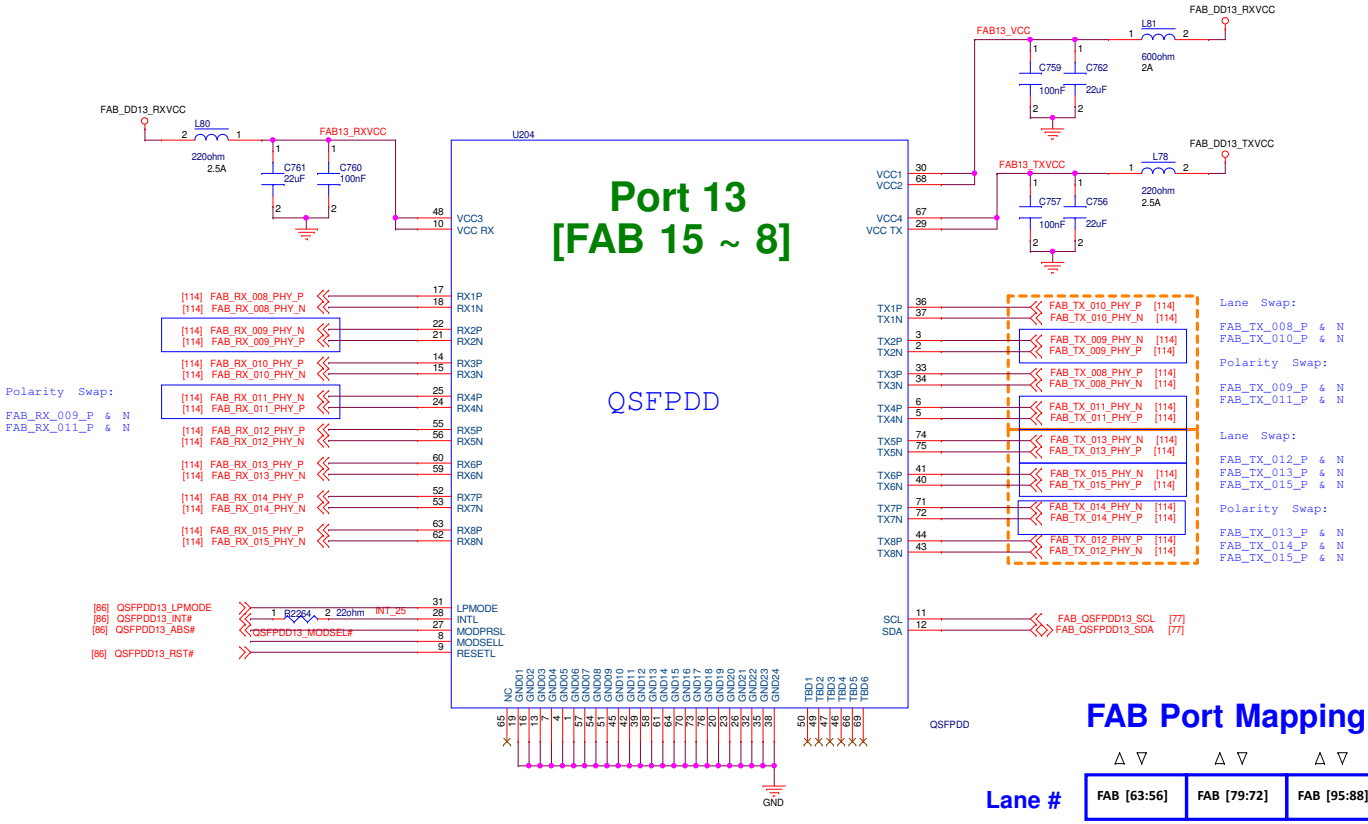
2.3 Blackhawk P/N Polarity Inversion

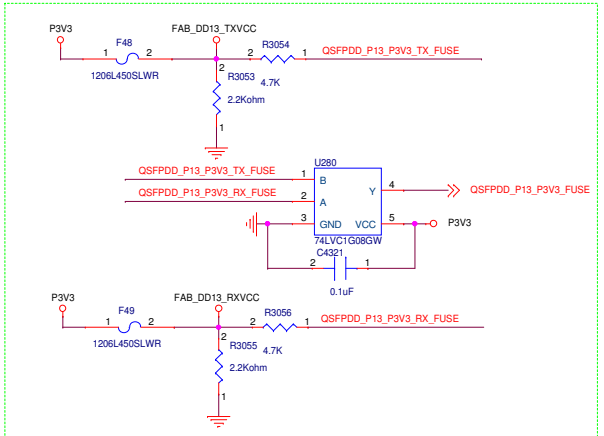
Blackhawk supports SerDes polarity inversion.

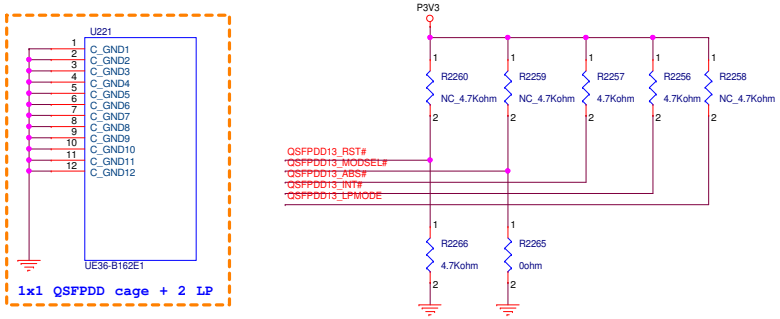
2.4.1 Blackhawk Lane Mapping – Fabric

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.







FAB Port Mapping

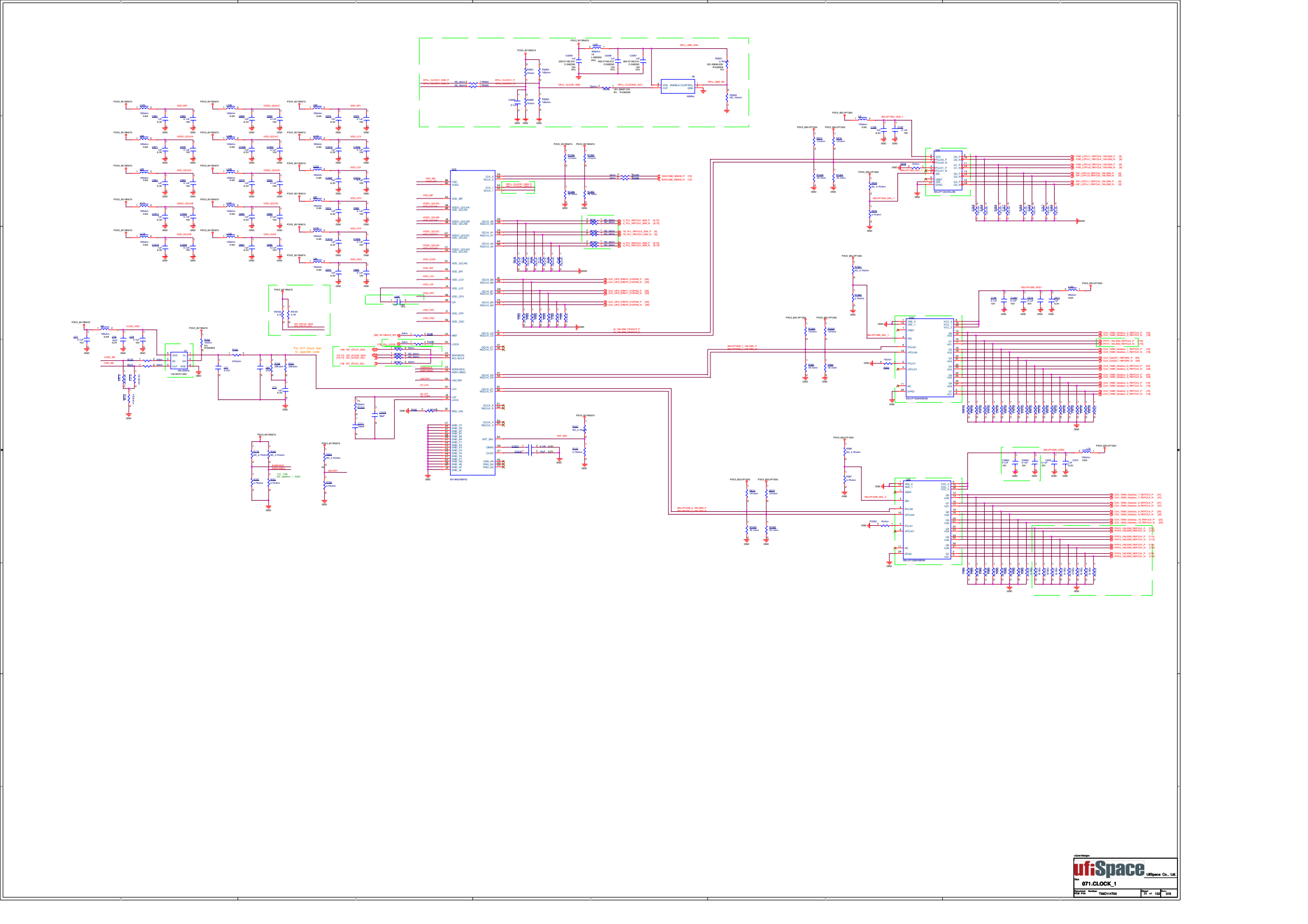
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	

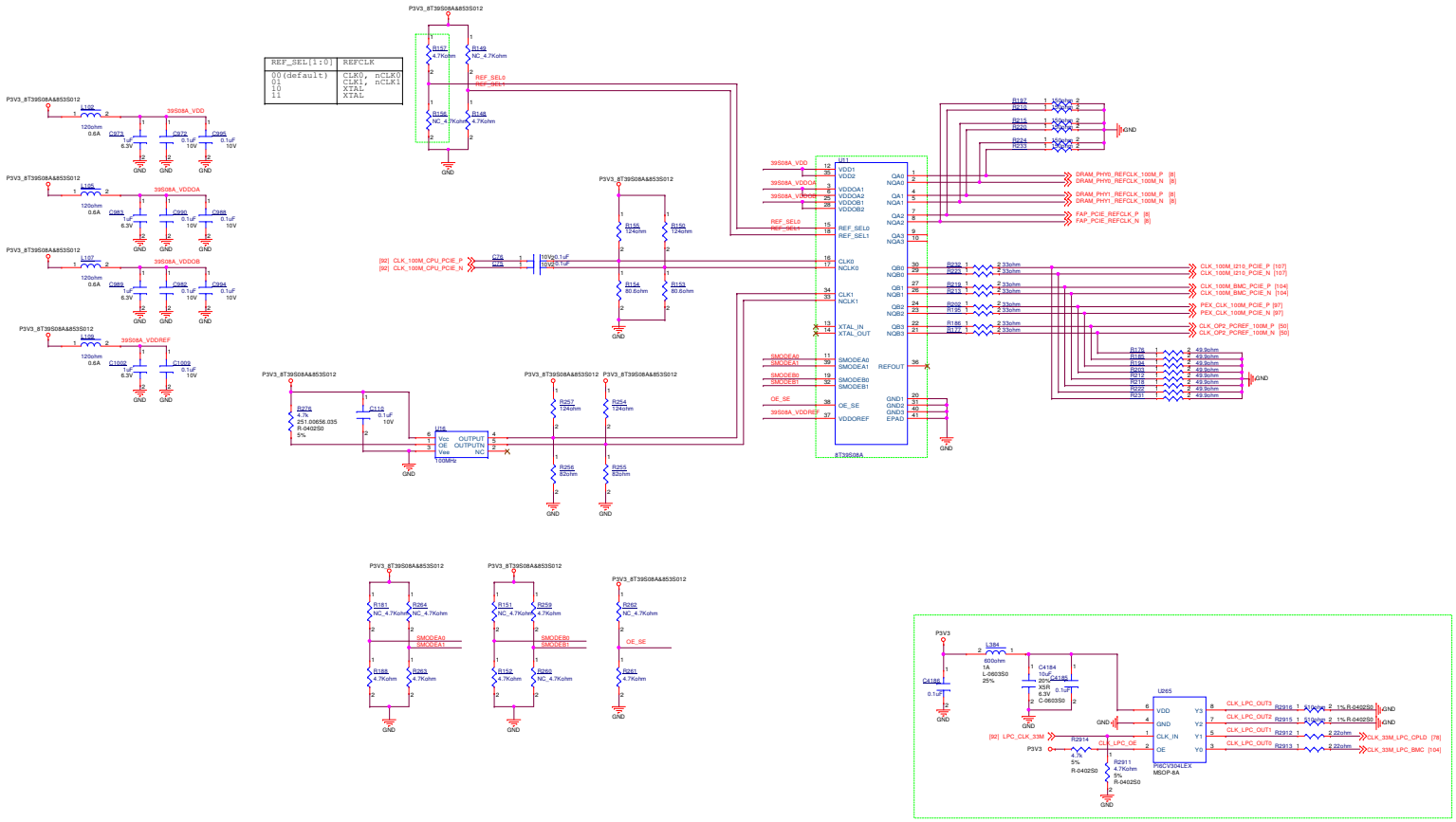
<Core Design>

UfiSpace Co., Ltd.

Title: 070_QSFPDD13

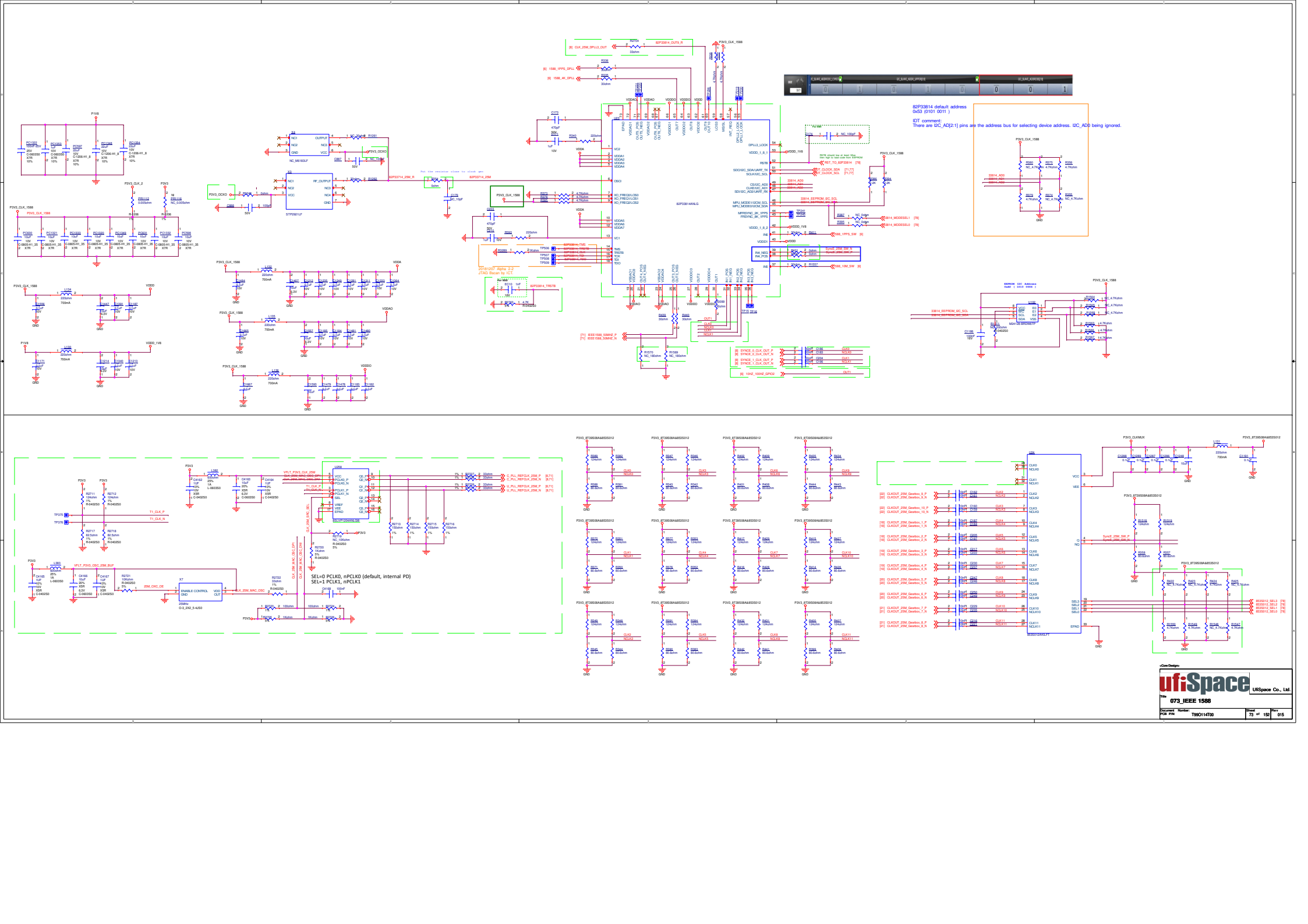
Document Number: T99O114T00 | Sheet 70 of 152 | Rev 015





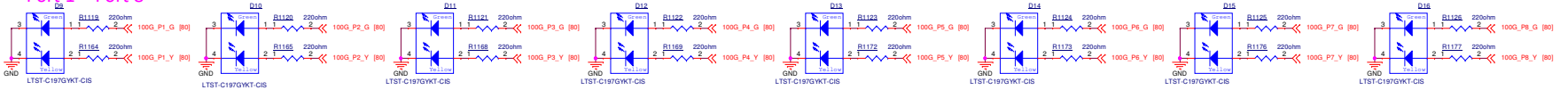
<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title	072.CLOCK_2		
Document Number: PCB P/N: T99O114T00		Sheet 72 of 152	Rev 015

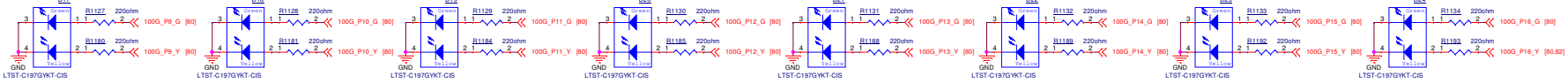

8ZP33814 default address
0x53 (0101 0011)
IDT comment:
There are I2C_AD[2:1] pins are the address bus for selecting device address. I2C_ADD being ignored.
SEL=0 PCLK0, nPCLK0 (default, internal PD)
SEL=1 PCLK1, nPCLK1
ufiSpace
UfiSpace Co., Ltd
073_IEEE 1588
T990114T00
Sheet 73 of 152
Rev 015

QSFP28

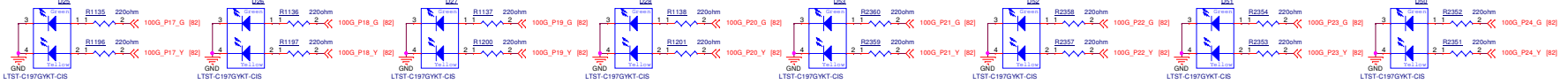
Port 1 ~ Port 8



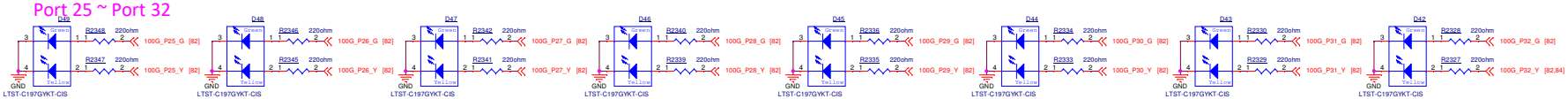
Port 9 ~ Port 16



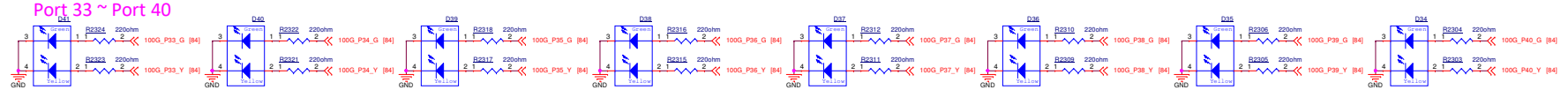
Port 17 ~ Port 24



Port 25 ~ Port 32



Port 33 ~ Port 40



QSFPDD

LED is actived-LOW

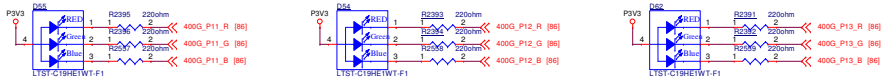
Port 1 ~ Port 4



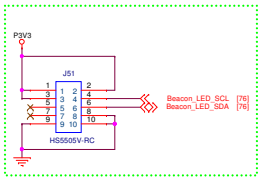
Port 5 ~ Port 10



Port 11 ~ Port 13



To LED BOARD CONNECTOR

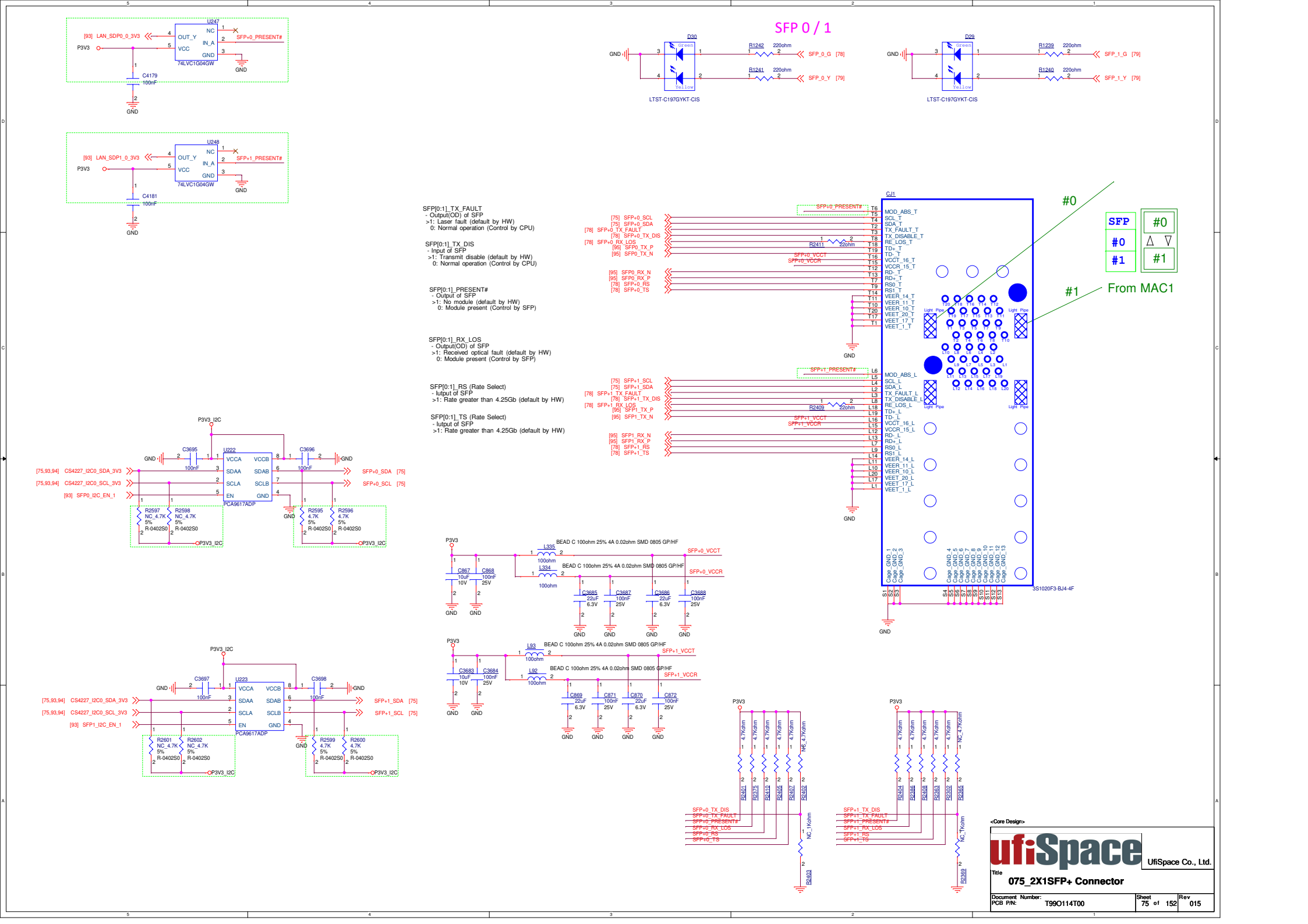


<Core Design>

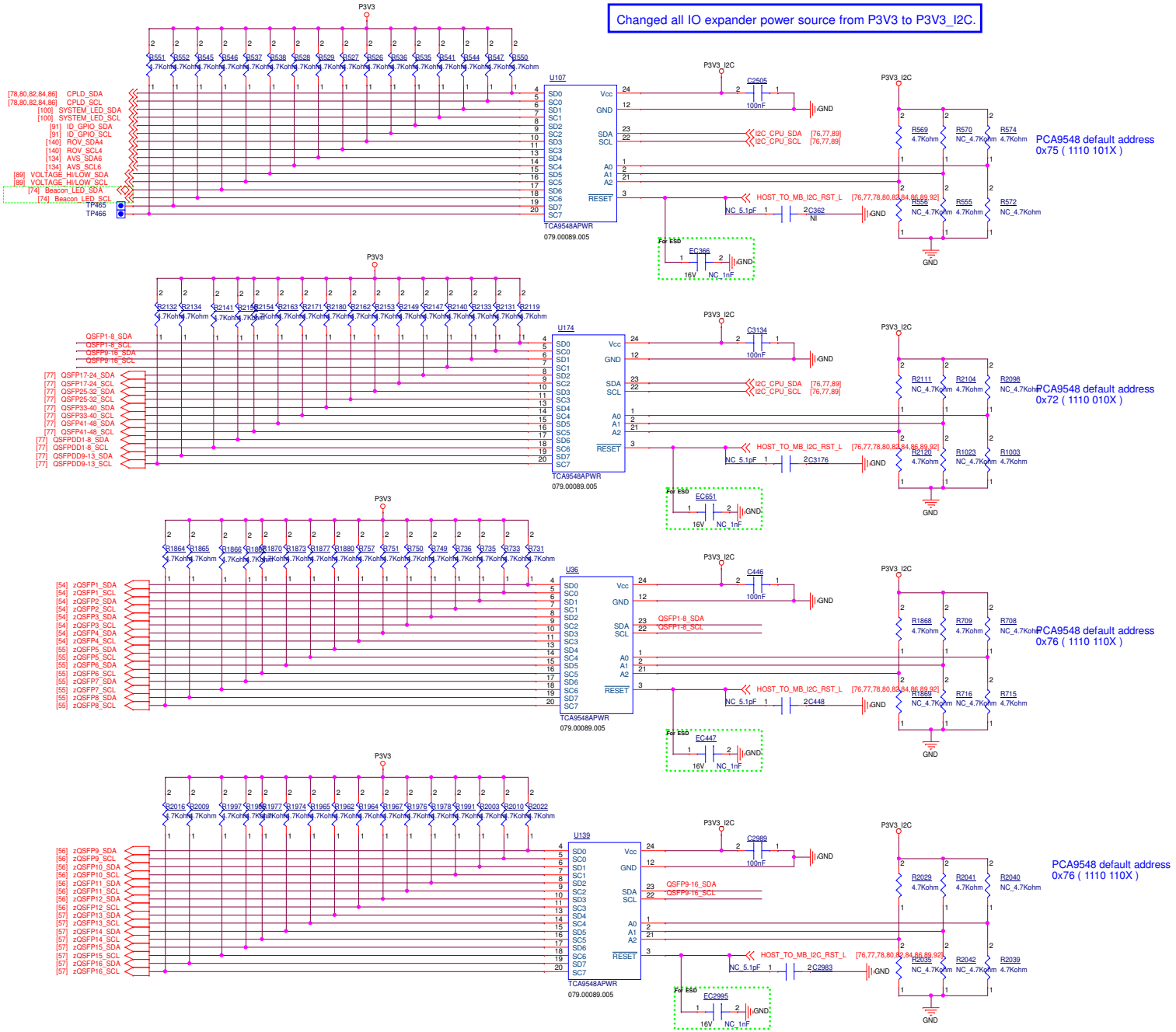
ufiSpace UfiSpace Co., Ltd.

Title: 074_LED CIRCUIT

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	74 of 152	015


SFP 0 / 1
U247
[93] LAN_SDP0_0_3V3
P3V3
OUT_Y
VCC
NC
IN_A
GND
74LVC1G04GW
SFP+0_PRESENT#
C4179
100nF
U248
[93] LAN_SDP1_0_3V3
SFP+1_PRESENT#
C4181
D30
D29
Green
Yellow
R1242
R1241
R1239
R1240
220ohm
SFP_0_G [78]
SFP_0_Y [79]
SFP_1_G [79]
SFP_1_Y [79]
LTST-C197GYKT-CIS
SFP[0:1]_TX_FAULT
- Output(OD) of SFP
>1: Laser fault (default by HW)
0: Normal operation (Control by CPU)
SFP[0:1]_TX_DIS
- Input of SFP
>1: Transmit disable (default by HW)
0: Normal operation (Control by CPU)
SFP[0:1]_PRESENT#
- Output of SFP
>1: No module (default by HW)
0: Module present (Control by SFP)
SFP[0:1]_RX_LOS
- Output(OD) of SFP
>1: Received optical fault (default by HW)
0: Module present (Control by SFP)
SFP[0:1]_RS (Rate Select)
- Iutput of SFP
>1: Rate greater than 4.25Gb (default by HW)
SFP[0:1]_TS (Rate Select)
- Iutput of SFP
>1: Rate greater than 4.25Gb (default by HW)
CJ1
MOD_ABS_T
SCL_T
SDA_T
TX_FAULT_T
TX_DISABLE_T
RE_LOS_T
TD+_T
TD-_T
VCCT_16_T
VCCR_15_T
RD-_T
RD+_T
RS0_T
RS1_T
VEER_14_T
VEER_11_T
VEER_10_T
VEET_20_T
VEET_17_T
VEET_1_T
MOD_ABS_L
SCL_L
SDA_L
TX_FAULT_L
TX_DISABLE_L
RE_LOS_L
TD+_L
TD-_L
VCCT_16_L
VCCR_15_L
RD-_L
RD+_L
RS0_L
RS1_L
VEER_14_L
VEER_11_L
VEER_10_L
VEET_20_L
VEET_17_L
VEET_1_L
SFP+0_PRESENT#
SFP+1_PRESENT#
SFP+0_VCCT
SFP+0_VCCR
SFP+1_VCCT
SFP+1_VCCR
R2411
R2409
220ohm
3S1020F3-BJ4-4F
#0
#1
From MAC1
SFP
#0
#1
U222
U223
P3V3_I2C
VCCA
VCCB
SDAA
SDAB
SCLA
SCLB
EN
GND
PCA9617ADP
C3695
C3696
C3697
C3698
100nF
[75,93,94] CS4227_I2C0_SDA_3V3
[75,93,94] CS4227_I2C0_SCL_3V3
[93] SFP0_I2C_EN_1
[93] SFP1_I2C_EN_1
SFP+0_SDA [75]
SFP+0_SCL [75]
SFP+1_SDA [75]
SFP+1_SCL [75]
R2597
R2598
R2595
R2596
R2601
R2602
R2599
R2600
NC_4.7K
4.7K
5%
R-0402S0
L335
L334
L93
L92
BEAD C 100ohm 25% 4A 0.02ohm SMD 0805 GP/HF
100ohm
C867
C868
C3683
C3684
10uF
10V
25V
C3685
C3687
C3686
C3688
22uF
6.3V
C869
C871
C870
C872
R2401
R2375
R2410
R2405
R2407
R2402
R2404
R2386
R2408
R2363
R2392
R2365
4.7Kohm
NC_4.7Kohm
NC_1Kohm
NC_7Kohm
R2403
R2393
SFP+0_TX_DIS
SFP+0_TX_FAULT
SFP+0_PRESENT#
SFP+0_RX_LOS
SFP+0_RS
SFP+0_TS
SFP+1_TX_DIS
SFP+1_TX_FAULT
SFP+1_PRESENT#
SFP+1_RX_LOS
SFP+1_RS
SFP+1_TS
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
075_2X1SFP+ Connector
Document Number:
PCB P/N:
T99O114T00
Sheet
75 of 152
Rev
015

Changed all IO expander power source from P3V3 to P3V3_I2C.



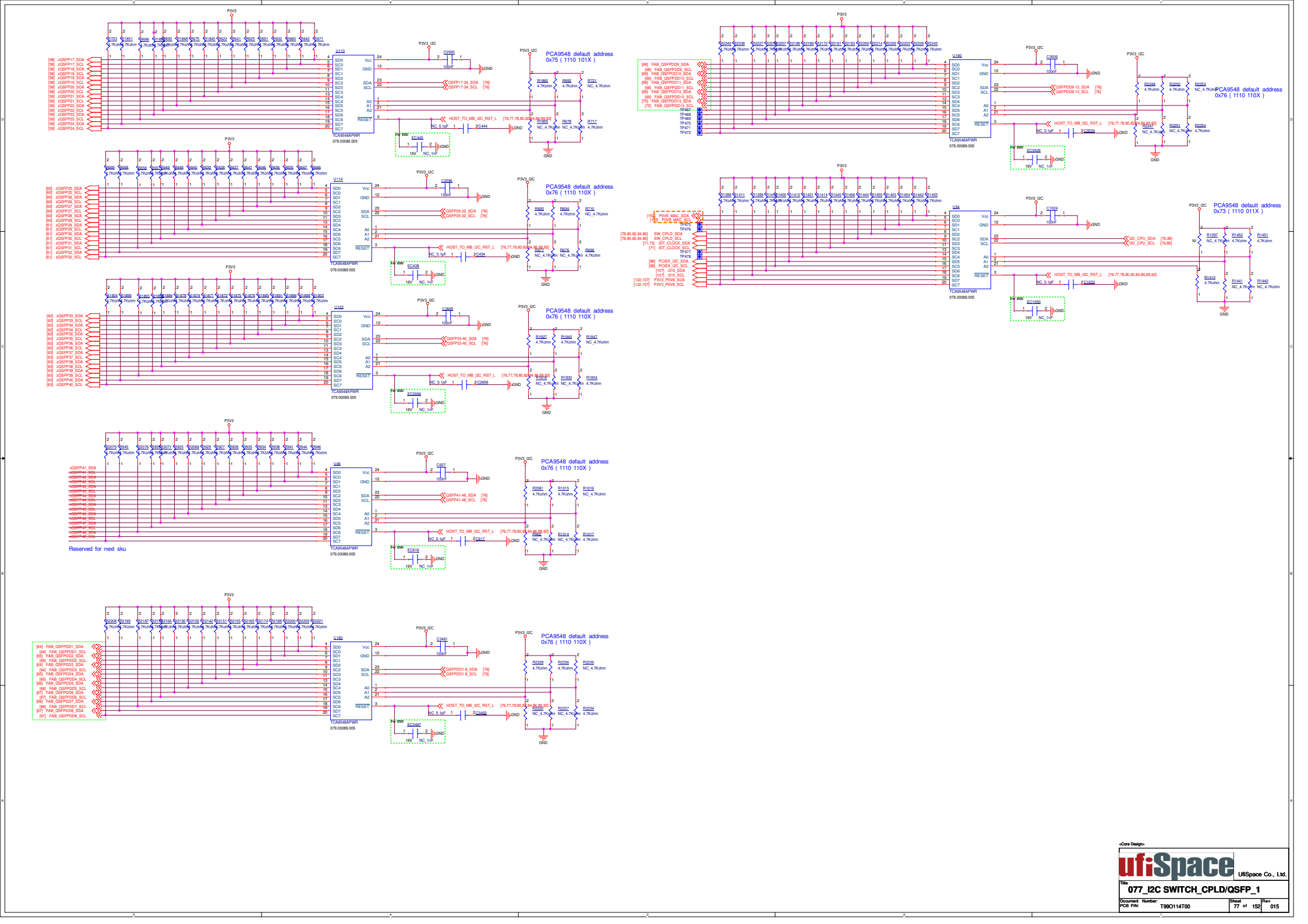
<Core Design>

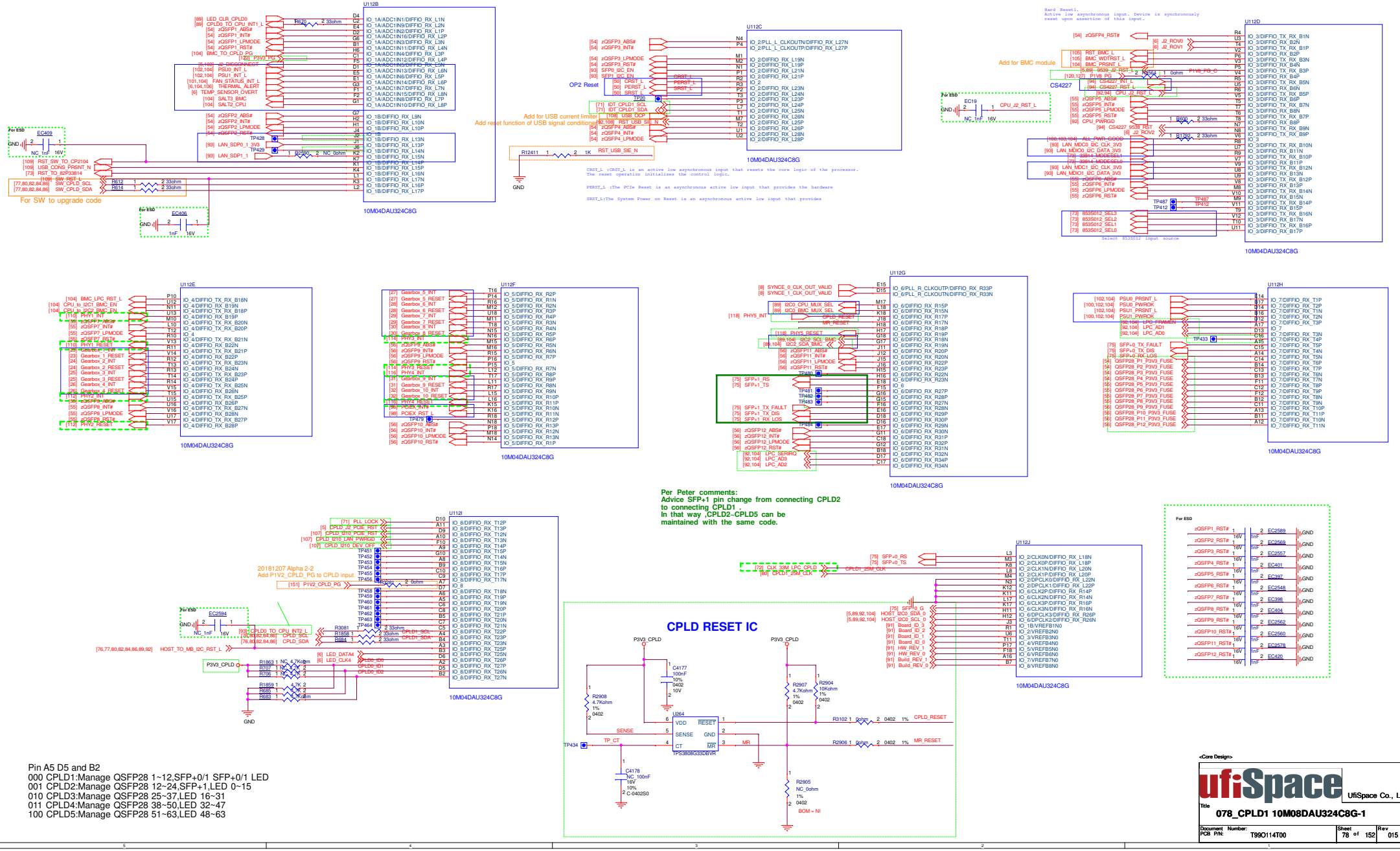
UfiSpace Co., Ltd.

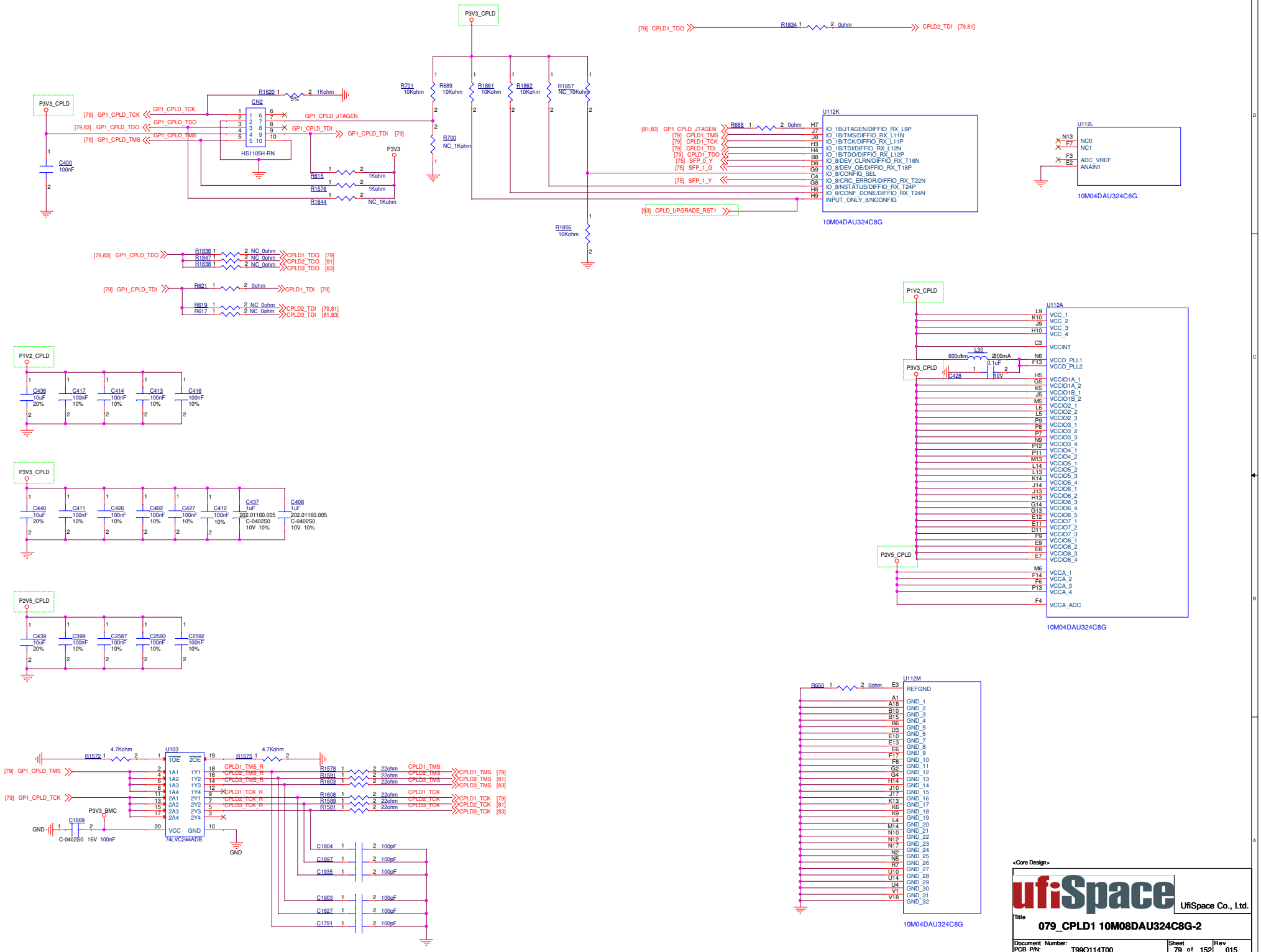
Title

076_I2C SWITCH_CPLD/QSFP_0

Document Number: PCB P/N: T99O114T00	Sheet 76 of 152	Rev 015


PCA9548 default address 0x75 (1110 101X)
PCA9548 default address 0x76 (1110 110X)
PCA9548 default address 0x73 (1110 011X)
Reserved for next sku
<Core Design>
ufiSpace
U6Space Co., Ltd.
Title
077_I2C SWITCH_CPLD/QSFP_1
Document Number:
PCB P/N:
T99O114T00
Sheet 77 of 152
Rev 015


U112B
U112C
U112D
U112E
U112F
U112G
U112H
U112I
U112J
10M04DAU324C8G
CPLD RESET IC
Per Peter comments:
Advice SFP+1 pin change from connecting CPLD2
to connecting CPLD1 .
In that way ,CPLD2~CPLD5 can be
maintained with the same code.
Add for BMC module
CS4227
Add for USB current limiter
Add reset function of USB signal conditioner
OP2 Reset
For SW to upgrade code
For ESD
20181207 Alpha 2-2
Add P1V2_CPLD_PG to CPLD input.
Pin A5 D5 and B2
000 CPLD1:Manage QSFP28 1~12,SFP+0/1 SFP+0/1 LED
001 CPLD2:Manage QSFP28 12~24,SFP+1,LED 0~15
010 CPLD3:Manage QSFP28 25~37,LED 16~31
011 CPLD4:Manage QSFP28 38~50,LED 32~47
100 CPLD5:Manage QSFP28 51~63,LED 48~63
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
078_CPLD1 10M08DAU324C8G-1
Document Number:
PCB P/N:
T990114T00
Sheet 78 of 152
Rev 015



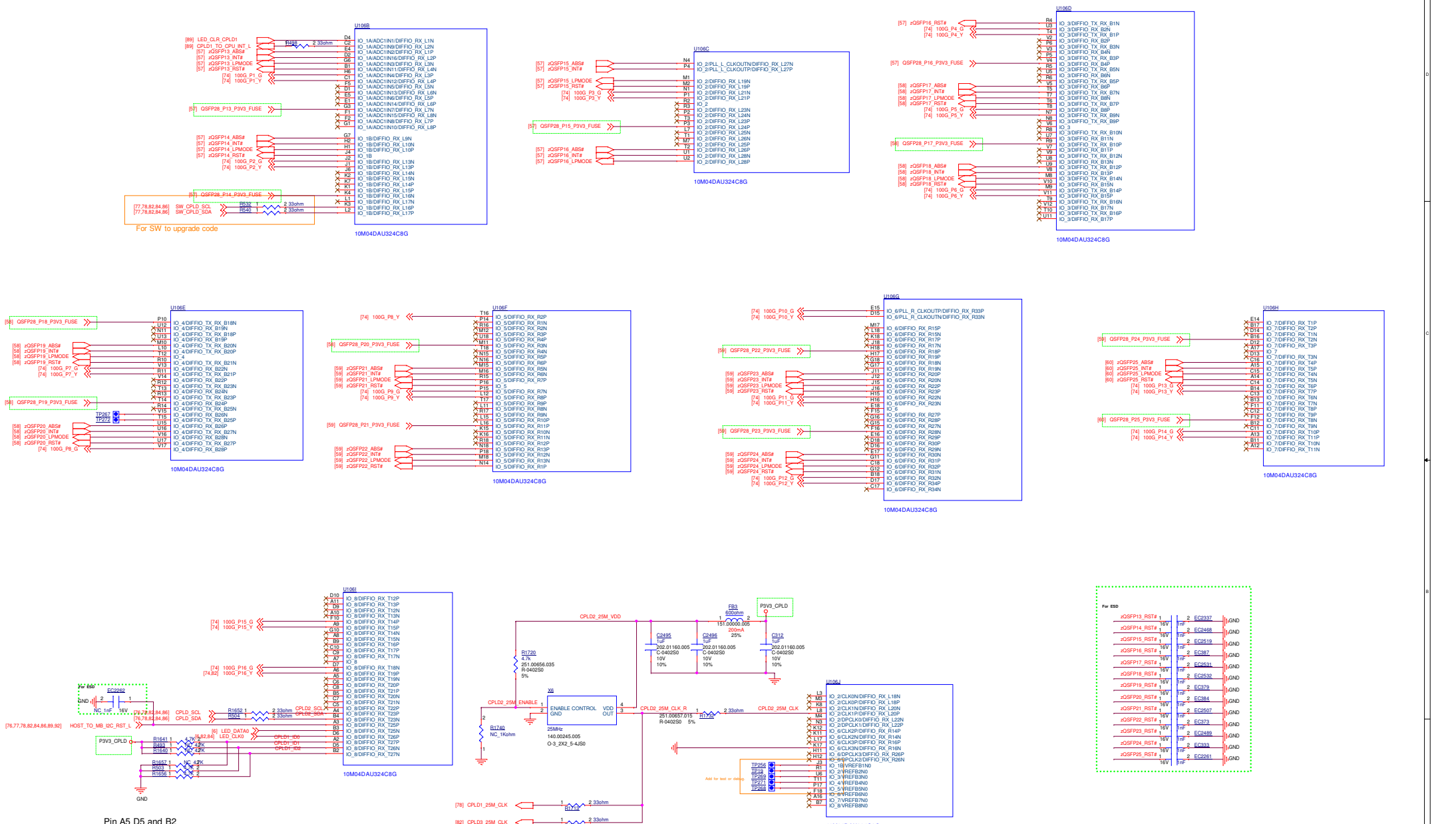
<Core Design>

UfiSpace Co., Ltd.

Title

079_CPLD1 10M08DAU324C8G-2

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	79 of 152	015

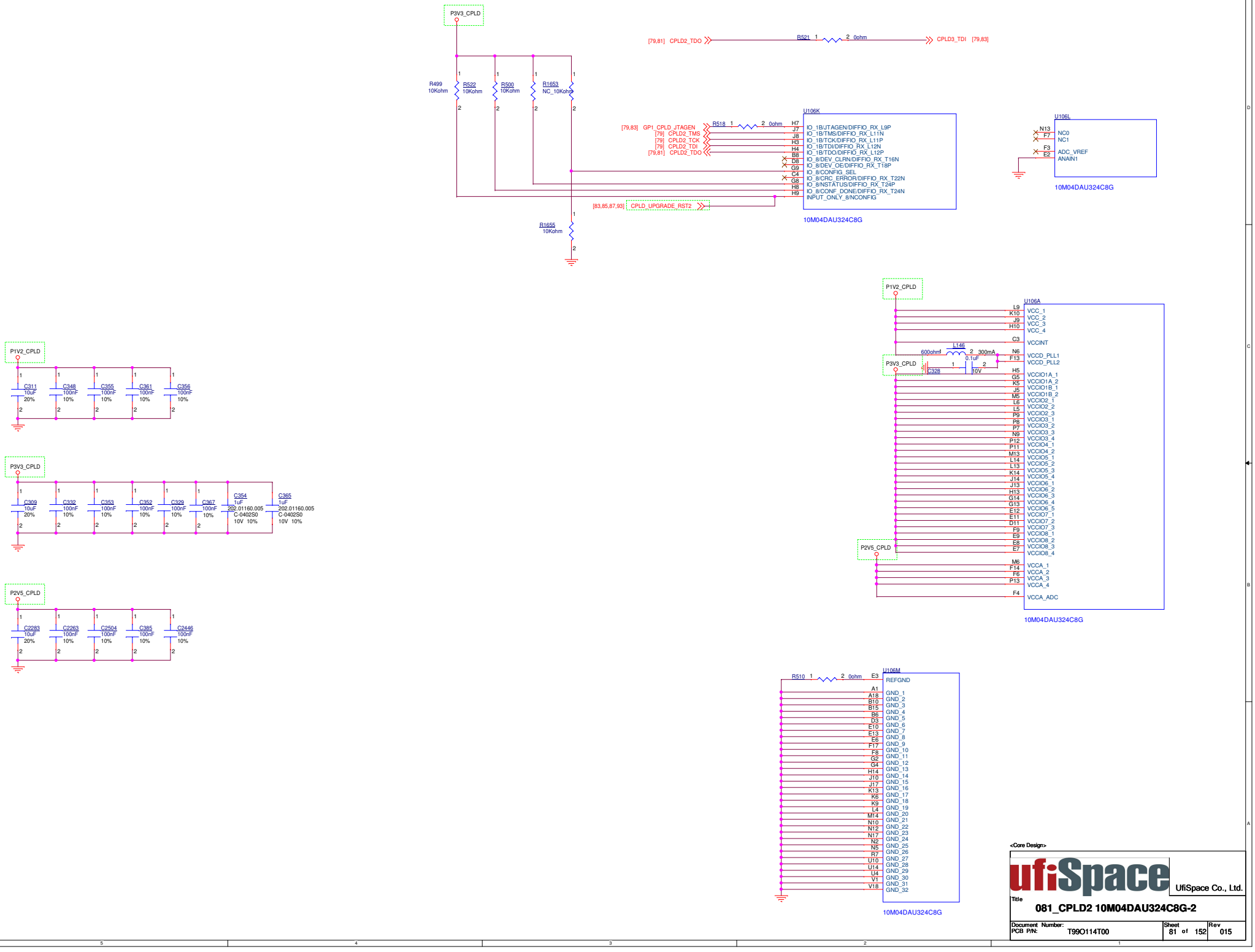


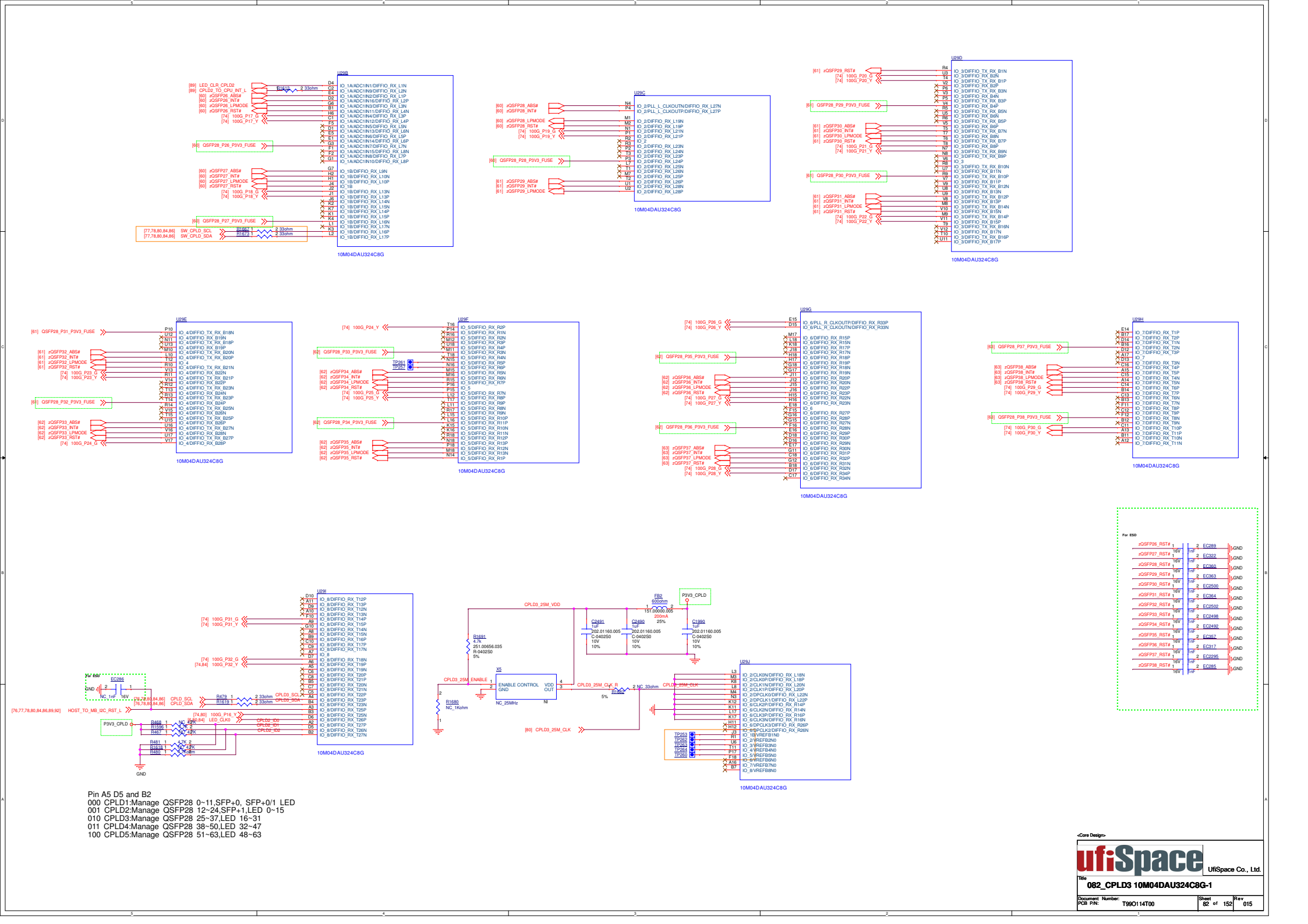
<Core Design>

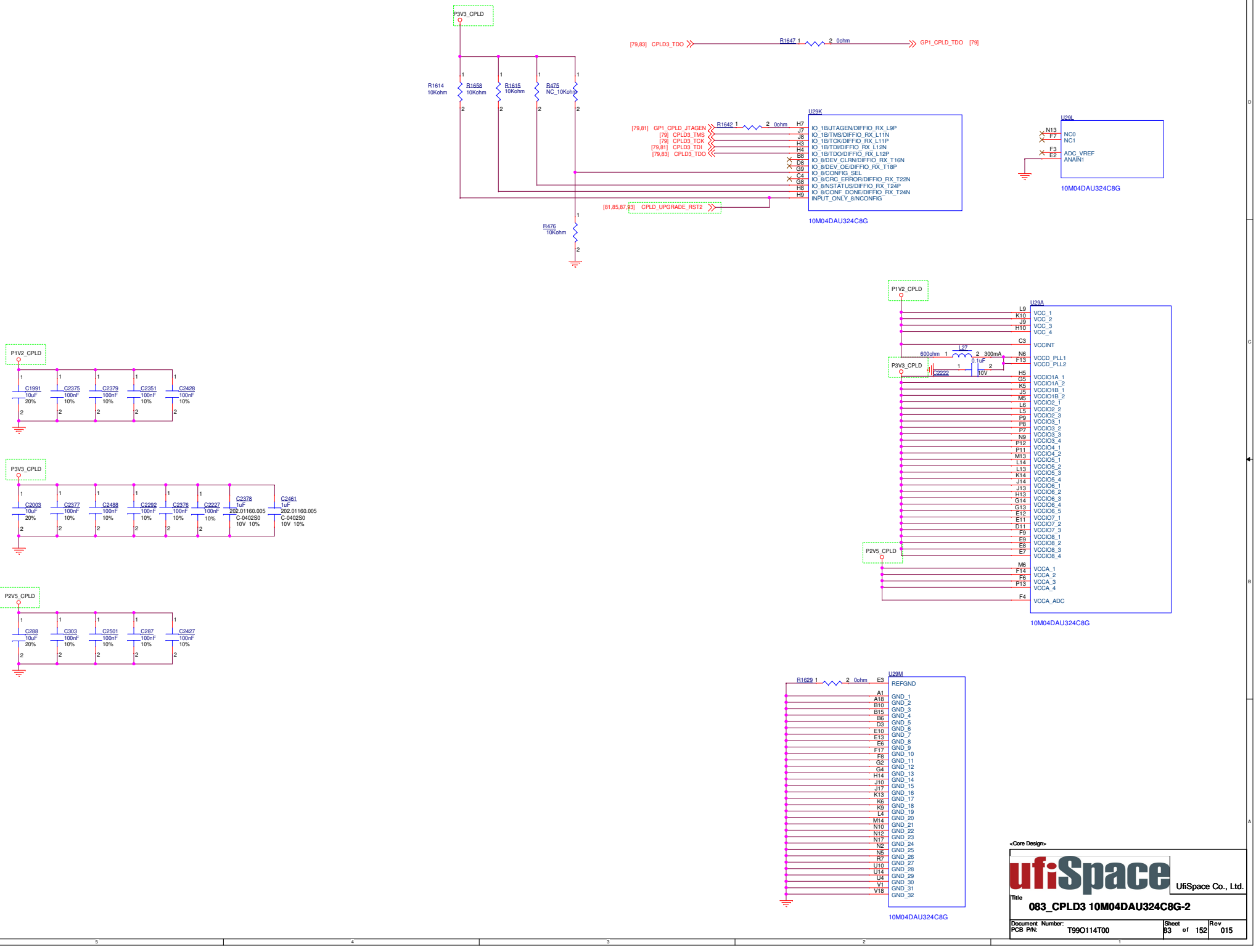
UfiSpace Co., Ltd.

Title: 080_CPLD2 10M04DAU324C8G-1

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	80 of 152	015


P3V3_CPLD
R499 10Kohm
R522 10Kohm
R500 10Kohm
R1653 NC_10Kohm
R1655 10Kohm
[79,81] CPLD2_TDO
R521 0ohm
CPLD3_TDI [79,83]
[79,83] GP1_CPLD_JTAGEN
R518 0ohm
[79] CPLD2_TMS
[79] CPLD2_TCK
[79] CPLD2_TDI
[79,81] CPLD2_TDO
[83,85,87,93] CPLD_UPGRADE_RST2
U106K
IO_1B/JTAGEN/DIFFIO_RX_L9P
IO_1B/TMS/DIFFIO_RX_L11N
IO_1B/TCK/DIFFIO_RX_L11P
IO_1B/TDI/DIFFIO_RX_L12N
IO_1B/TDO/DIFFIO_RX_L12P
IO_8/DEV_CLRN/DIFFIO_RX_T16N
IO_8/DEV_OE/DIFFIO_RX_T18P
IO_8/CONFIG_SEL
IO_8/CRC_ERROR/DIFFIO_RX_T22N
IO_8/NSTATUS/DIFFIO_RX_T24P
IO_8/CONF_DONE/DIFFIO_RX_T24N
INPUT_ONLY_8/NCONFIG
10M04DAU324C8G
U106L
NC0
NC1
ADC_VREF
ANAIN1
10M04DAU324C8G
P1V2_CPLD
C311 10uF 20%
C348 100nF 10%
C355 100nF 10%
C361 100nF 10%
C356 100nF 10%
P3V3_CPLD
C309 10uF 20%
C332 100nF 10%
C353 100nF 10%
C352 100nF 10%
C329 100nF 10%
C367 100nF 10%
C354 1uF 202.01160.005 C-0402S0 10V 10%
C365 1uF 202.01160.005 C-0402S0 10V 10%
P2V5_CPLD
C2283 10uF 20%
C2263 100nF 10%
C2504 100nF 10%
C385 100nF 10%
C2446 100nF 10%
P1V2_CPLD
L146 600ohm 300mA
P3V3_CPLD
C328 0.1uF 10V
P2V5_CPLD
U106A
VCC_1
VCC_2
VCC_3
VCC_4
VCCINT
VCCD_PLL1
VCCD_PLL2
VCCIO1A_1
VCCIO1A_2
VCCIO1B_1
VCCIO1B_2
VCCIO2_1
VCCIO2_2
VCCIO2_3
VCCIO3_1
VCCIO3_2
VCCIO3_3
VCCIO3_4
VCCIO4_1
VCCIO4_2
VCCIO5_1
VCCIO5_2
VCCIO5_3
VCCIO5_4
VCCIO6_1
VCCIO6_2
VCCIO6_3
VCCIO6_4
VCCIO6_5
VCCIO7_1
VCCIO7_2
VCCIO7_3
VCCIO8_1
VCCIO8_2
VCCIO8_3
VCCIO8_4
VCCA_1
VCCA_2
VCCA_3
VCCA_4
VCCA_ADC
10M04DAU324C8G
R510 0ohm
U106M
REFGND
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
10M04DAU324C8G
<Core Design>
UfiSpace Co., Ltd.
Title
081_CPLD2 10M04DAU324C8G-2
Document Number:
PCB P/N: T99O114T00
Sheet 81 of 152
Rev 015


U29B
U29C
U29D
U29E
U29F
U29G
U29H
U29I
U29J
10M04DAU324C8G
Pin A5 D5 and B2
000 CPLD1:Manage QSFP28 0~11,SFP+0, SFP+0/1 LED
001 CPLD2:Manage QSFP28 12~24,SFP+1,LED 0~15
010 CPLD3:Manage QSFP28 25~37,LED 16~31
011 CPLD4:Manage QSFP28 38~50,LED 32~47
100 CPLD5:Manage QSFP28 51~63,LED 48~63
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
082_CPLD3 10M04DAU324C8G-1
Document Number:
PCB P/N: T99O114T00
Sheet 82 of 152
Rev 015

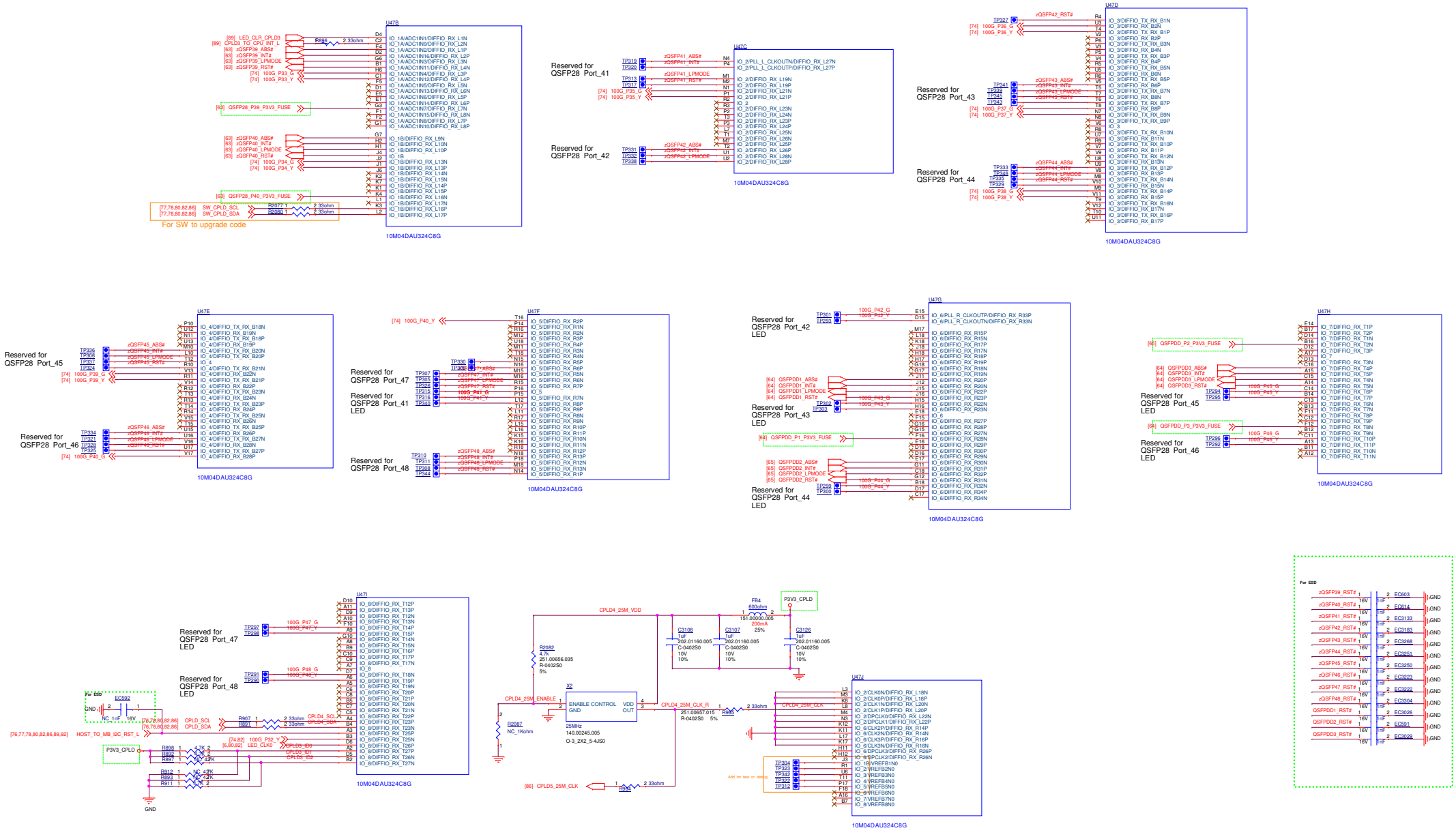


<Core Design>

UfiSpace Co., Ltd.

Title: 083_CPLD3 10M04DAU324C8G-2

Document Number:		Sheet		Rev
PCB P/N: T99O114T00		83	of 152	015



<Core Design>

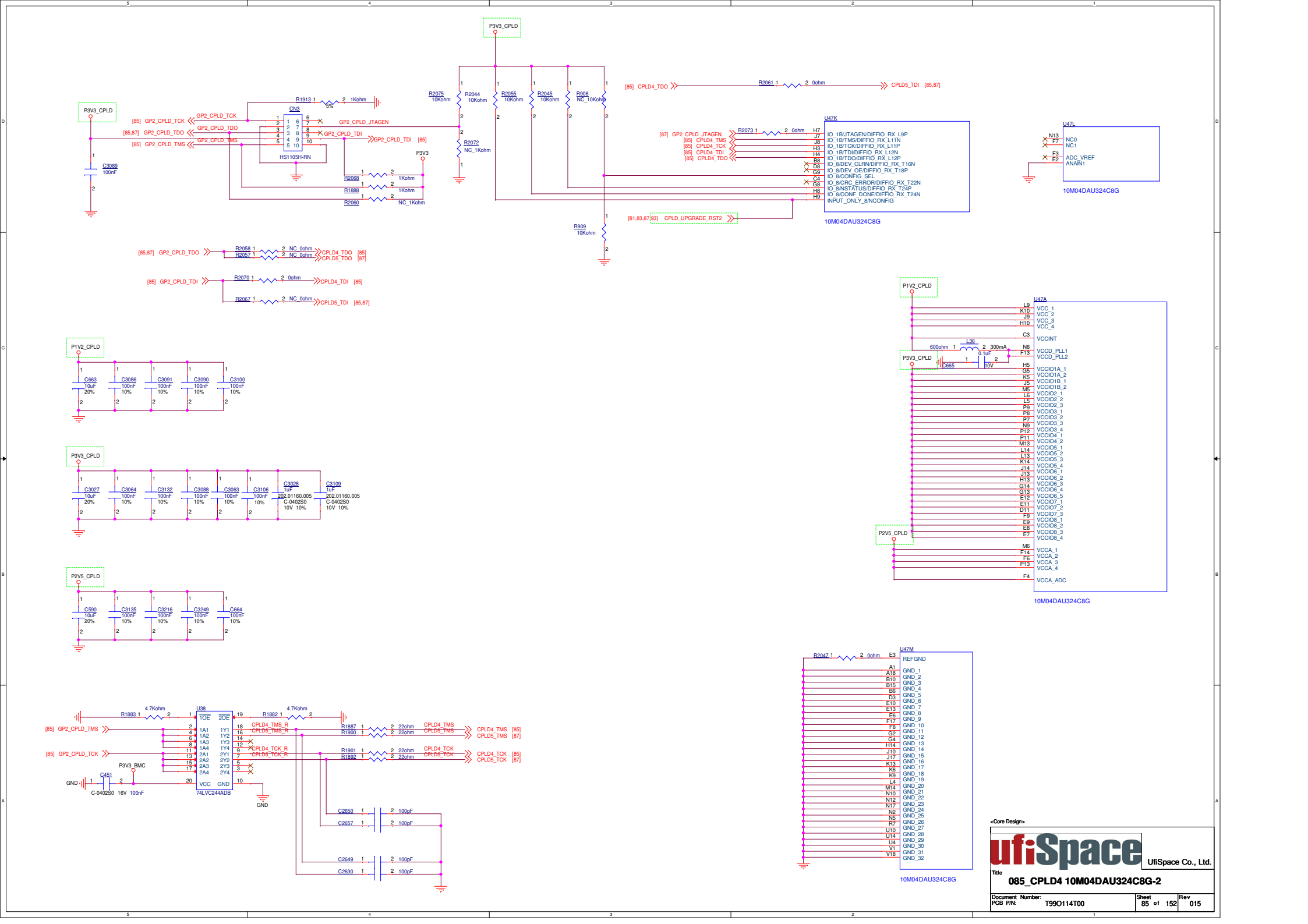
ufiSpace

UfiSpace Co., Ltd.

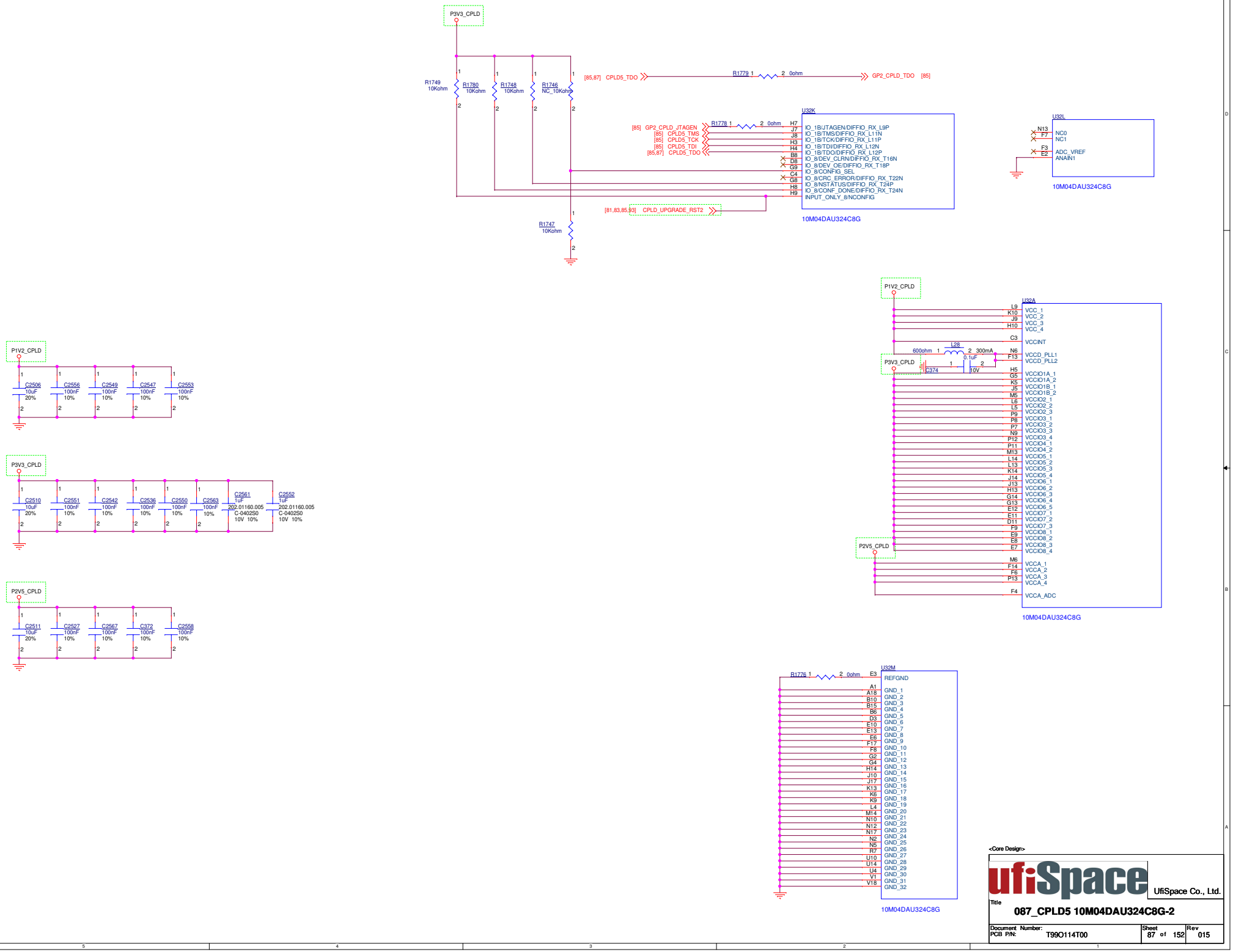
Title

084_CPLD4 10M04DAU324C8G-1

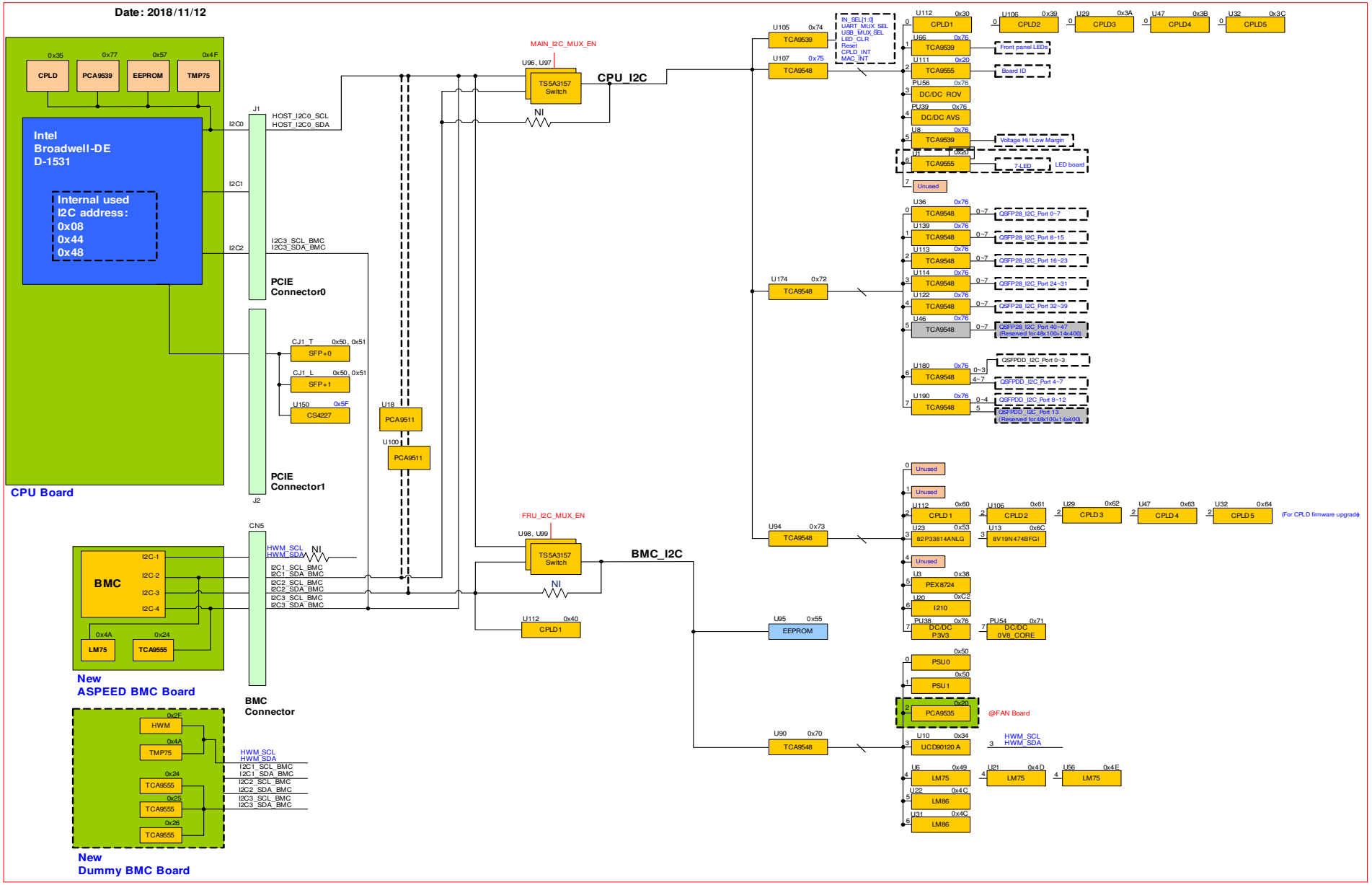
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	84 of 152	015


P3V3_CPLD
R2075 10Kohm
R2044 10Kohm
R2055 10Kohm
R2045 10Kohm
R908 NC_10Kohm
R909 10Kohm
R2072 NC_1Kohm
[85] CPLD4_TDO
R2061 0ohm
CPLD5_TDI [85,87]
P3V3_CPLD
[85] GP2_CPLD_TCK
[85,87] GP2_CPLD_TDO
[85] GP2_CPLD_TMS
R1913 1Kohm 5%
CN3
HS1105H-RN
GP2_CPLD_JTAGEN
GP2_CPLD_TDI
GP2_CPLD_TDI [85]
C3089 100nF
R2068 1Kohm
R1888 1Kohm
R2060 NC_1Kohm
P3V3
[87] GP2_CPLD_JTAGEN
[85] CPLD4_TMS
[85] CPLD4_TCK
[85] CPLD4_TDI
[85] CPLD4_TDO
R2073 0ohm
U47K
IO_1B/JTAGEN/DIFFIO_RX_L9P
IO_1B/TMS/DIFFIO_RX_L11N
IO_1B/TCK/DIFFIO_RX_L11P
IO_1B/TDI/DIFFIO_RX_L12N
IO_1B/TDO/DIFFIO_RX_L12P
IO_8/DEV_CLRN/DIFFIO_RX_T16N
IO_8/DEV_OE/DIFFIO_RX_T18P
IO_8/CONFIG_SEL
IO_8/CRC_ERROR/DIFFIO_RX_T22N
IO_8/NSTATUS/DIFFIO_RX_T24P
IO_8/CONF_DONE/DIFFIO_RX_T24N
INPUT_ONLY_8/NCONFIG
10M04DAU324C8G
[81,83,93] CPLD_UPGRADE_RST2
U47L
NC0
NC1
ADC_VREF
ANAIN1
10M04DAU324C8G
[85,87] GP2_CPLD_TDO
R2058 NC_0ohm
R2057 NC_0ohm
CPLD4_TDO [85]
CPLD5_TDO [87]
[85] GP2_CPLD_TDI
R2070 0ohm
CPLD4_TDI [85]
R2067 NC_0ohm
CPLD5_TDI [85,87]
P1V2_CPLD
C663 10uF 20%
C3086 100nF 10%
C3091 100nF 10%
C3090 100nF 10%
C3100 100nF 10%
P3V3_CPLD
C3027 10uF 20%
C3064 100nF 10%
C3132 100nF 10%
C3088 100nF 10%
C3063 100nF 10%
C3106 100nF 10%
C3028 1uF 202.01160.005 C-0402S0 10V 10%
C3109 1uF 202.01160.005 C-0402S0 10V 10%
P2V5_CPLD
C590 10uF 20%
C3135 100nF 10%
C3216 100nF 10%
C3249 100nF 10%
C664 100nF 10%
P1V2_CPLD
U47A
VCC_1
VCC_2
VCC_3
VCC_4
VCCINT
600ohm L36 300mA
VCCD_PLL1
VCCD_PLL2
P3V3_CPLD
C665 0.1uF 10V
VCCIO1A_1
VCCIO1A_2
VCCIO1B_1
VCCIO1B_2
VCCIO2_1
VCCIO2_2
VCCIO2_3
VCCIO3_1
VCCIO3_2
VCCIO3_3
VCCIO3_4
VCCIO4_1
VCCIO4_2
VCCIO5_1
VCCIO5_2
VCCIO5_3
VCCIO5_4
VCCIO6_1
VCCIO6_2
VCCIO6_3
VCCIO6_4
VCCIO6_5
VCCIO7_1
VCCIO7_2
VCCIO7_3
VCCIO8_1
VCCIO8_2
VCCIO8_3
VCCIO8_4
P2V5_CPLD
VCCA_1
VCCA_2
VCCA_3
VCCA_4
VCCA_ADC
10M04DAU324C8G
[85] GP2_CPLD_TMS
[85] GP2_CPLD_TCK
R1883 4.7Kohm
R1882 4.7Kohm
U38
74LVC244ADB
CPLD4_TMS_R
CPLD5_TMS_R
CPLD4_TCK_R
CPLD5_TCK_R
R1887 22ohm
R1900 22ohm
R1901 22ohm
R1892 22ohm
CPLD4_TMS
CPLD5_TMS
CPLD4_TCK
CPLD5_TCK
CPLD4_TMS [85]
CPLD5_TMS [87]
CPLD4_TCK [85]
CPLD5_TCK [87]
P3V3_BMC
C451 C-0402S0 16V 100nF
GND
C2650 100pF
C2657 100pF
C2649 100pF
C2630 100pF
R2047 0ohm
U47M
REFGND
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
10M04DAU324C8G
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
085_CPLD4 10M04DAU324C8G-2
Document Number:
PCB P/N: T99O114T00
Sheet 85 of 152
Rev 015

U32B
10M04DAU324C8G
For SW to upgrade code
U32C
10M04DAU324C8G
U32D
10M04DAU324C8G
U32E
10M04DAU324C8G
U32F
10M04DAU324C8G
U32G
10M04DAU324C8G
Reserved for QSFPDD Port_14
U32H
10M04DAU324C8G
Reserved for QSFPDD Port_14 LED
U32I
10M04DAU324C8G
U32J
10M04DAU324C8G
For ESD
Pin A5 D5 and B2
000 CPLD1:Manage QSFP28 0~11,SFP+0, SFP+0/1 LED
001 CPLD2:Manage QSFP28 12~24,SFP+1,LED 0~15
010 CPLD3:Manage QSFP28 25~37,LED 16~31
011 CPLD4:Manage QSFP28 38~50,LED 32~47
100 CPLD5:Manage QSFP28 51~63,LED 48~63
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
086_CPLD5 10M04DAU324C8G-1
Document Number:
PCB P/N: T99O114T00
Sheet 86 of 152
Rev 015


P3V3_CPLD
R1749 10Kohm
R1780 10Kohm
R1748 10Kohm
R1746 NC_10Kohm
R1747 10Kohm
[85,87] CPLD5_TDO
R1779 0ohm
GP2_CPLD_TDO [85]
U32K
[85] GP2_CPLD_JTAGEN
R1778 0ohm
[85] CPLD5_TMS
[85] CPLD5_TCK
[85] CPLD5_TDI
[85,87] CPLD5_TDO
H7 IO_1B/JTAGEN/DIFFIO_RX_L9P
J7 IO_1B/TMS/DIFFIO_RX_L11N
J8 IO_1B/TCK/DIFFIO_RX_L11P
H3 IO_1B/TDI/DIFFIO_RX_L12N
H4 IO_1B/TDO/DIFFIO_RX_L12P
B8 IO_8/DEV_CLRN/DIFFIO_RX_T16N
D8 IO_8/DEV_OE/DIFFIO_RX_T18P
G9 IO_8/CONFIG_SEL
C4 IO_8/CRC_ERROR/DIFFIO_RX_T22N
G8 IO_8/NSTATUS/DIFFIO_RX_T24P
H8 IO_8/CONF_DONE/DIFFIO_RX_T24N
H9 INPUT_ONLY_8/NCONFIG
[81,83,85,93] CPLD_UPGRADE_RST2
10M04DAU324C8G
U32L
N13 NC0
F7 NC1
F3 ADC_VREF
E2 ANAIN1
10M04DAU324C8G
P1V2_CPLD
C2506 10uF 20%
C2556 100nF 10%
C2549 100nF 10%
C2547 100nF 10%
C2553 100nF 10%
P3V3_CPLD
C2510 10uF 20%
C2551 100nF 10%
C2542 100nF 10%
C2536 100nF 10%
C2550 100nF 10%
C2563 100nF 10%
C2561 1uF 202.01160.005 C-0402S0 10V 10%
C2552 1uF 202.01160.005 C-0402S0 10V 10%
P2V5_CPLD
C2511 10uF 20%
C2527 100nF 10%
C2567 100nF 10%
C372 100nF 10%
C2558 100nF 10%
P1V2_CPLD
P3V3_CPLD
L28 600ohm 300mA
0.1uF 10V
C374
P2V5_CPLD
U32A
L9 VCC_1
K10 VCC_2
J9 VCC_3
H10 VCC_4
C3 VCCINT
N6 VCCD_PLL1
F13 VCCD_PLL2
H5 VCCIO1A_1
G5 VCCIO1A_2
K5 VCCIO1B_1
J5 VCCIO1B_2
M5 VCCIO2_1
L6 VCCIO2_2
L5 VCCIO2_3
P9 VCCIO3_1
P8 VCCIO3_2
P7 VCCIO3_3
N9 VCCIO3_4
P12 VCCIO4_1
P11 VCCIO4_2
M13 VCCIO5_1
L14 VCCIO5_2
L13 VCCIO5_3
K14 VCCIO5_4
J14 VCCIO6_1
J13 VCCIO6_2
H13 VCCIO6_3
G14 VCCIO6_4
G13 VCCIO6_5
E12 VCCIO7_1
E11 VCCIO7_2
D11 VCCIO7_3
F9 VCCIO8_1
E9 VCCIO8_2
E8 VCCIO8_3
E7 VCCIO8_4
M6 VCCA_1
F14 VCCA_2
F6 VCCA_3
P13 VCCA_4
F4 VCCA_ADC
10M04DAU324C8G
R1776 0ohm
U32M
E3 REFGND
A1 GND_1
A18 GND_2
B10 GND_3
B15 GND_4
B6 GND_5
D3 GND_6
E10 GND_7
E13 GND_8
E6 GND_9
F17 GND_10
F8 GND_11
G2 GND_12
G4 GND_13
H14 GND_14
J10 GND_15
J17 GND_16
K13 GND_17
K6 GND_18
K9 GND_19
L4 GND_20
M14 GND_21
N10 GND_22
N12 GND_23
N17 GND_24
N2 GND_25
N5 GND_26
R7 GND_27
U10 GND_28
U14 GND_29
U4 GND_30
V1 GND_31
V18 GND_32
10M04DAU324C8G
<Core Design>
ufiSpace
UfiSpace Co., Ltd.
Title
087_CPLD5 10M04DAU324C8G-2
Document Number:
PCB P/N: T99O114T00
Sheet 87 of 152
Rev 015

Date: 2018/11/12

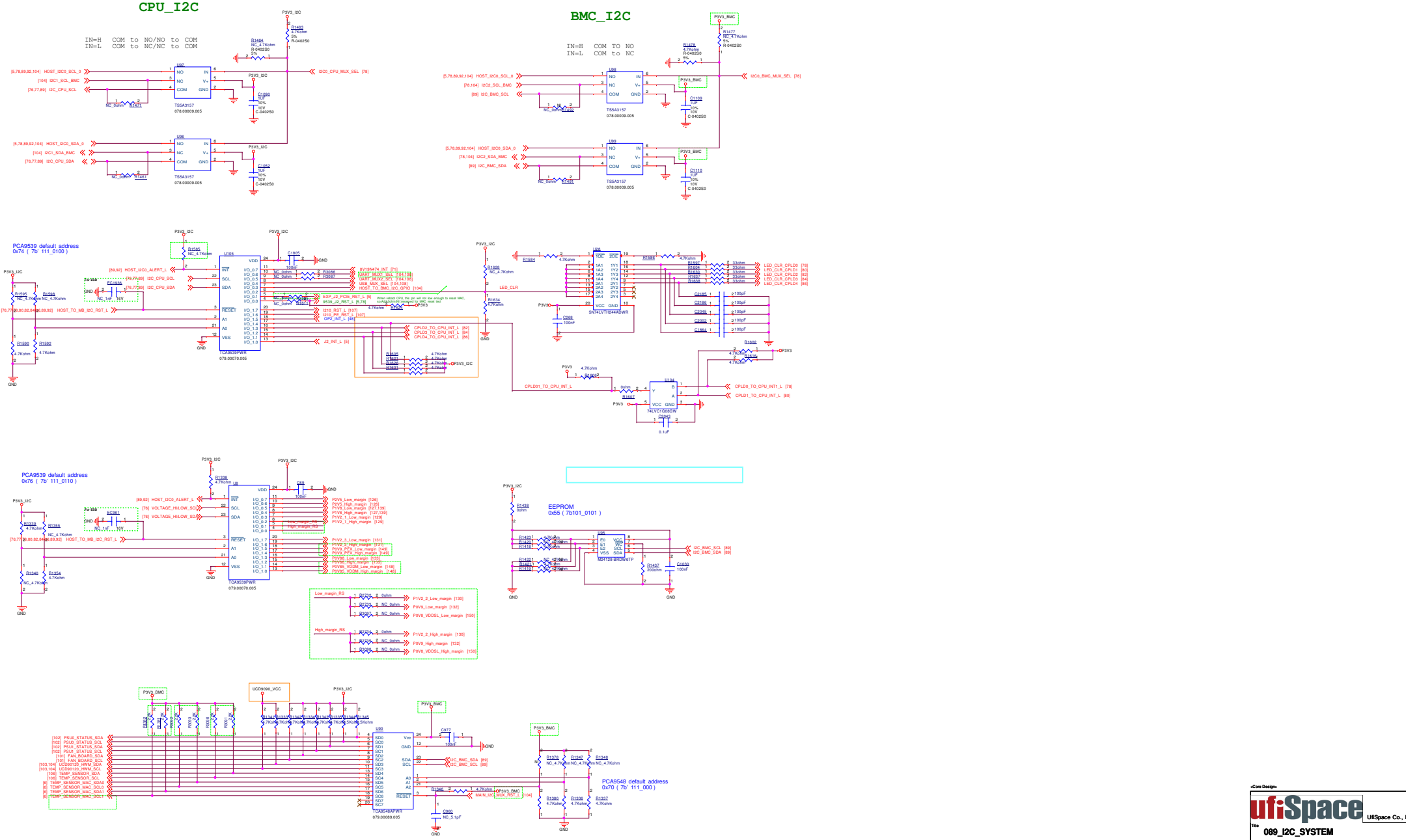


<Core Design>

UfiSpace Co., Ltd.

Title: 088_I2C DIAGRAM

Document Number: PCB P/N: T99O114T00	Sheet 88 of 152	Rev 015



<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title: 089_I2C_SYSTEM

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	89 of 152	015

MOUNTING HOLE

Mounting Hole = 3.5mm

H25 H30 H26 H31 H24 H32 H4 H5 — Hole-3.5mm — GND GND

H33 H28 H15 H12 H29 H11 H7 H34 H9 — Hole-3.5mm — GND GND

H10 H23 H18 H21 H22 H19 H20 H14 H17 — Hole-3.5mm — GND GND

H35 H16 H13 — Hole-3.5mm — GND GND

H6 H40 — Hole-3.5mm — GND GND

H27 H8 — Hole-4.6mm — GND GND

PAD1
480.01302.005
Thermal pad

PAD2
480.01303.005
Thermal pad

BOM ONLY PARTS

PCB1
304.01007.015
PCB

LABEL1
503.01032.005
LABEL

LABEL2
503.01032.005
LABEL

LABEL3
503.01032.005
LABEL

LABEL
503.01032.005
LABEL

COVER1
426.05394.005
COVER

FRAME1
432.00718.005
FRAME

HEATSINK1
400.00747.015
PEX8724 Heatsink

OCXO SHIELDING COVER HOLES

H38 H39 H37 H36 — Hole-1.2X2.2 MPTH24X79R48X103

R3082 0ohm
R3083 0ohm
R3084 0ohm
R3085 0ohm

H3 NON_PTH_HOLE_9.5MM

H2 NON_PTH_HOLE_8.4MM

H1 NON_PTH_HOLE_9.5MM

<Core Design>

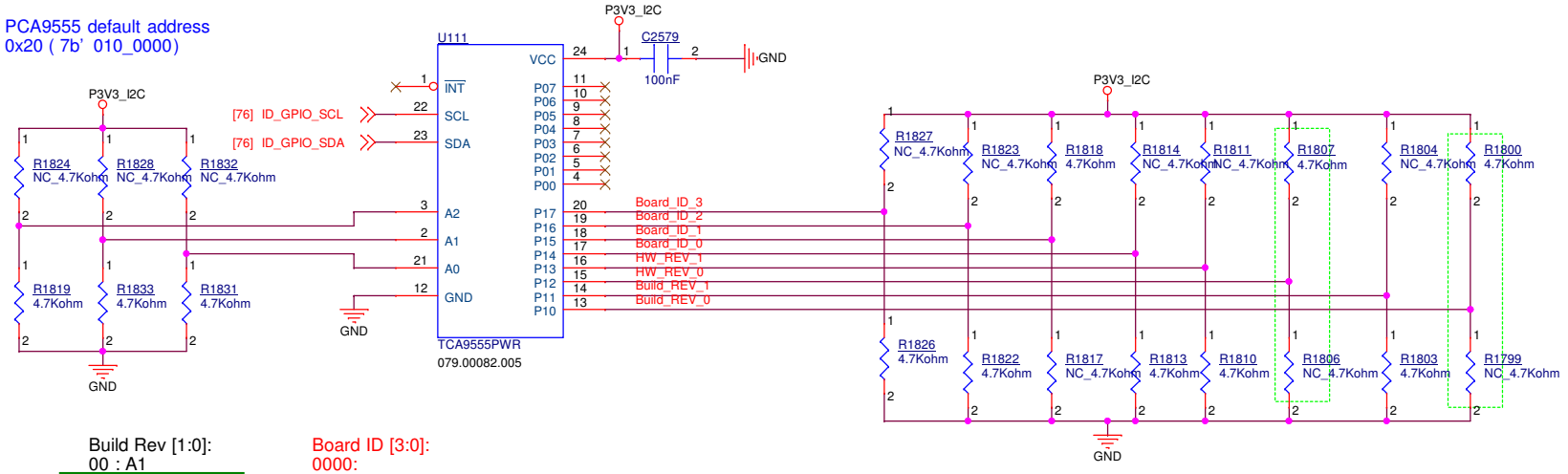
ufiSpace UfiSpace Co., Ltd.

Title: 090_SCREW

Document Number: T99O114T00
PCB P/N:

Sheet 90 of 152

Rev 015



Build Rev [1:0]:
00 : A1
01 : A2
10 : A3
11 : A4

Hardware Revision [1:0]:
Proto : 00
Alpha : 01
Beta : 10
PVT : 11

Board ID [3:0]:
0000:
0001:
0010:NCP1-1
0011:
0100:
0101:
0110:
0111:
1000:
1001:

1010~1111: Reserved

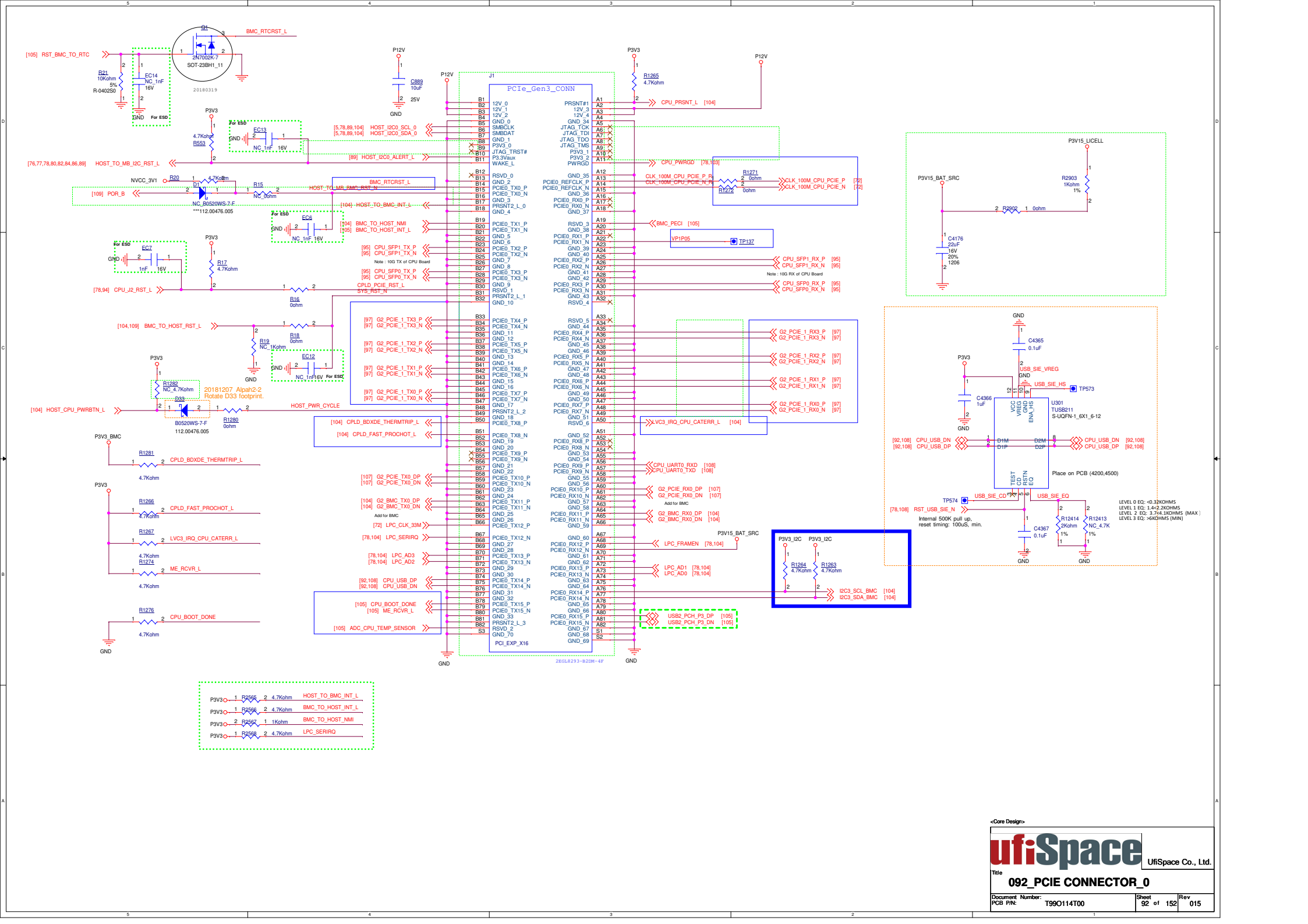
Board_ID_3 Board_ID_3 [78]
Board_ID_2 Board_ID_2 [78]
Board_ID_1 Board_ID_1 [78]
Board_ID_0 Board_ID_0 [78]
HW_REV_1 HW_REV_1 [78]
HW_REV_0 HW_REV_0 [78]
Build_REV_1 Build_REV_1 [78]
Build_REV_0 Build_REV_0 [78]

<Core Design>

UfiSpace Co., Ltd.

Title
091_SWITCH INT

Document Number: PCB P/N: T99O114T00	Sheet 91 of 152	Rev 015

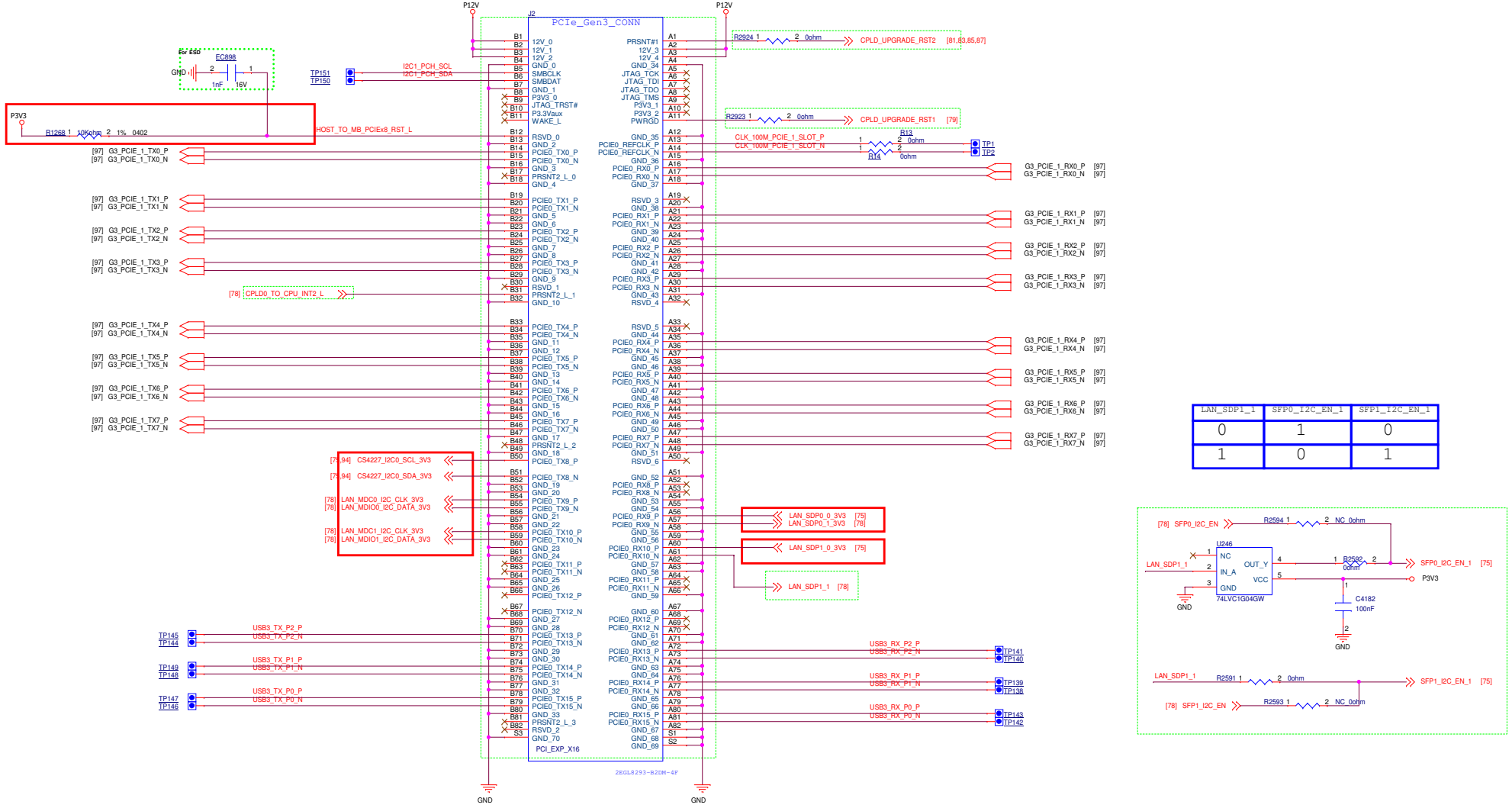


<Core Design>

UfiSpace Co., Ltd.

Title: 092_PCIE CONNECTOR_0

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	92 of 152	015



LAN_SDP1_1	SFP0_I2C_EN_1	SFP1_I2C_EN_1
0	1	0
1	0	1

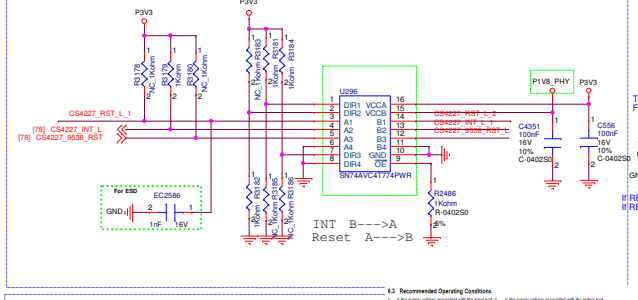
<Core Design>

UfiSpace Co., Ltd.

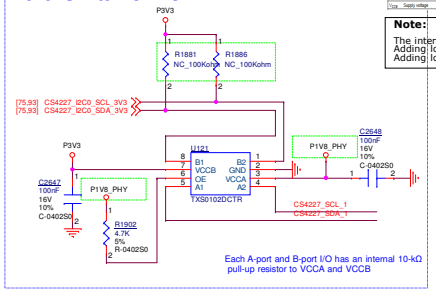
Title: 093_PCIE CONNECTOR_1

Document Number: PCB P/N: T99O114T00	Sheet 93 of 152	Rev 015

Level Shifter for INT / RESET



Level Shifter for I2C



6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

	MIN	MAX	UNIT
V_{CCA} Supply voltage[1]	1.65	3.6	V
V_{CCB} Supply voltage	2.3	5.5	V

Note:
The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.

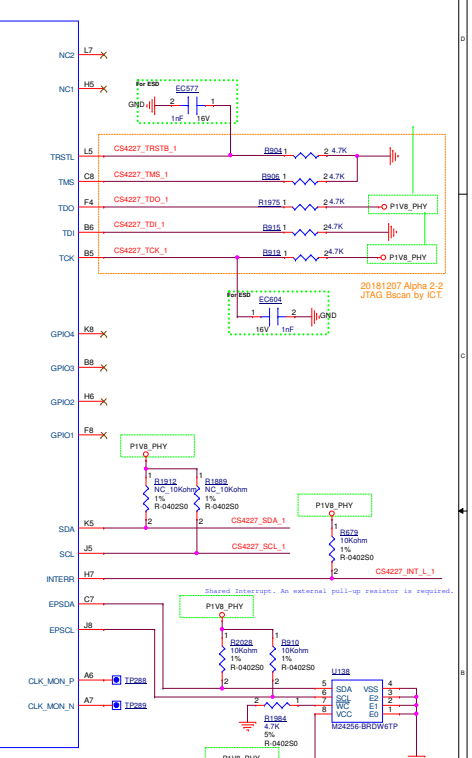
MICROSEL1	MICROSEL0	MODE
1	0	MDIO
0	1	I2C
0	0	I2C (Fast)

Tie to 1.8 V for 1.2 V I/O voltage levels
Float or tie to 0 V for 1.8 V/2.5 V I/O voltage levels

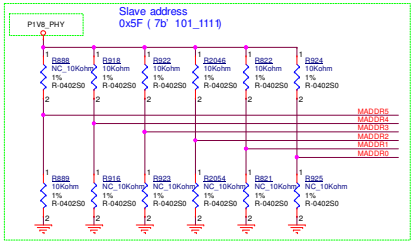
If REF_CLK exceeds 180 MHz, then tie REFDIV2_ENB low.
If REF_CLK is 180 MHz or less, tie REFDIV2_ENB high.

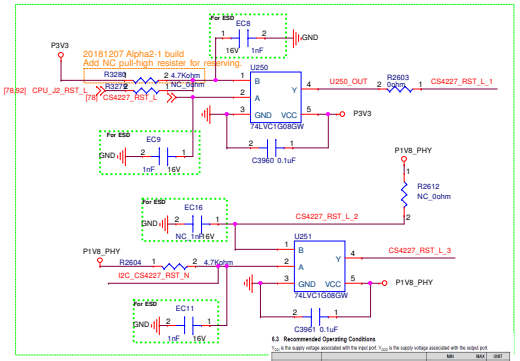
The CS4227 PHY reference clock inputs REF_CLK_P/N may be connected directly to a differential source (without AC coupling capacitors) provided the specified Input Voltage Range (Table 45) is not exceeded for either the P or N inputs.

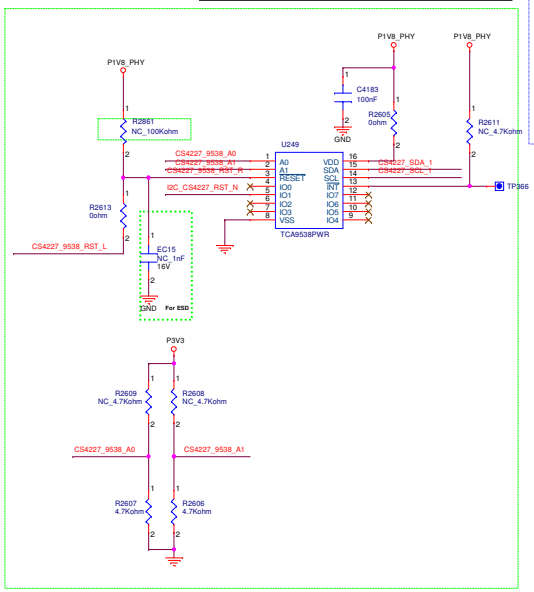
CONTROL



Slave address
0x5F (7b' 101_1111)







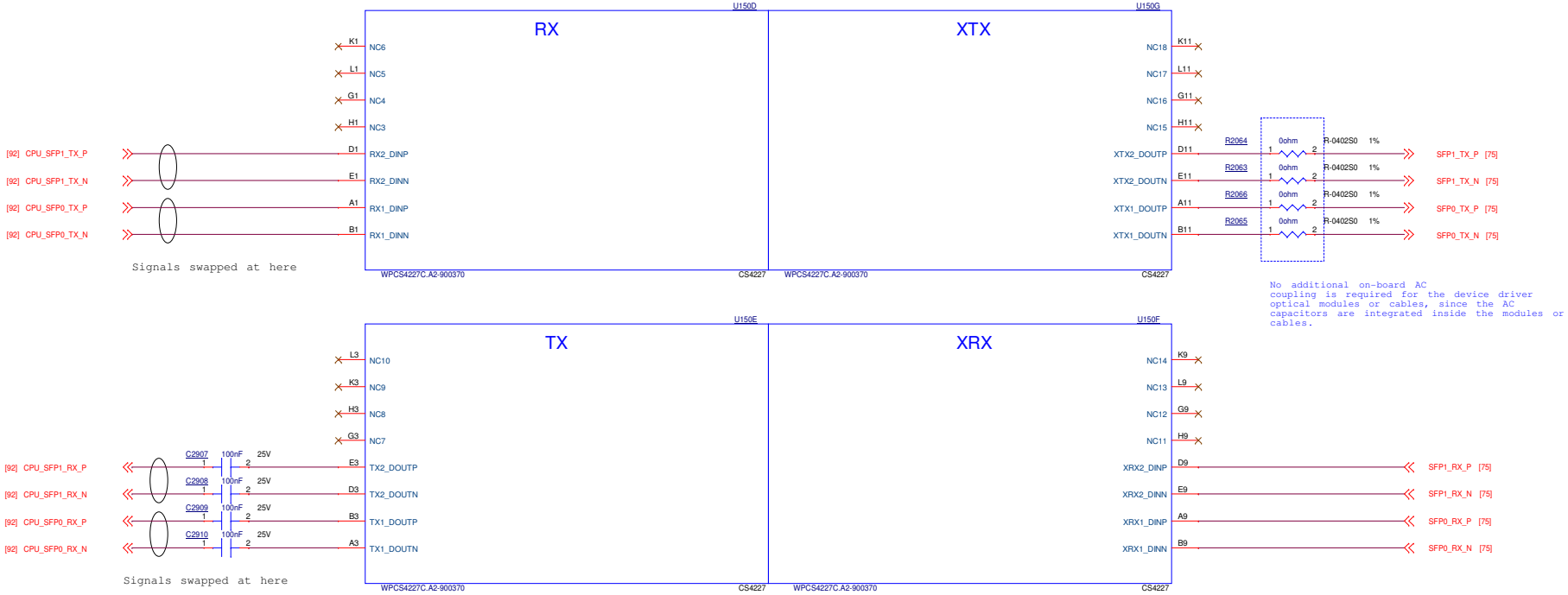
<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title
094_CS4227_RESET_CLK_JTAG

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	94 of 152	015

Line Data (From CPU)

Host Data (To SFP+)



No additional on-board AC coupling is required for the device driver optical modules or cables, since the AC capacitors are integrated inside the modules or cables.

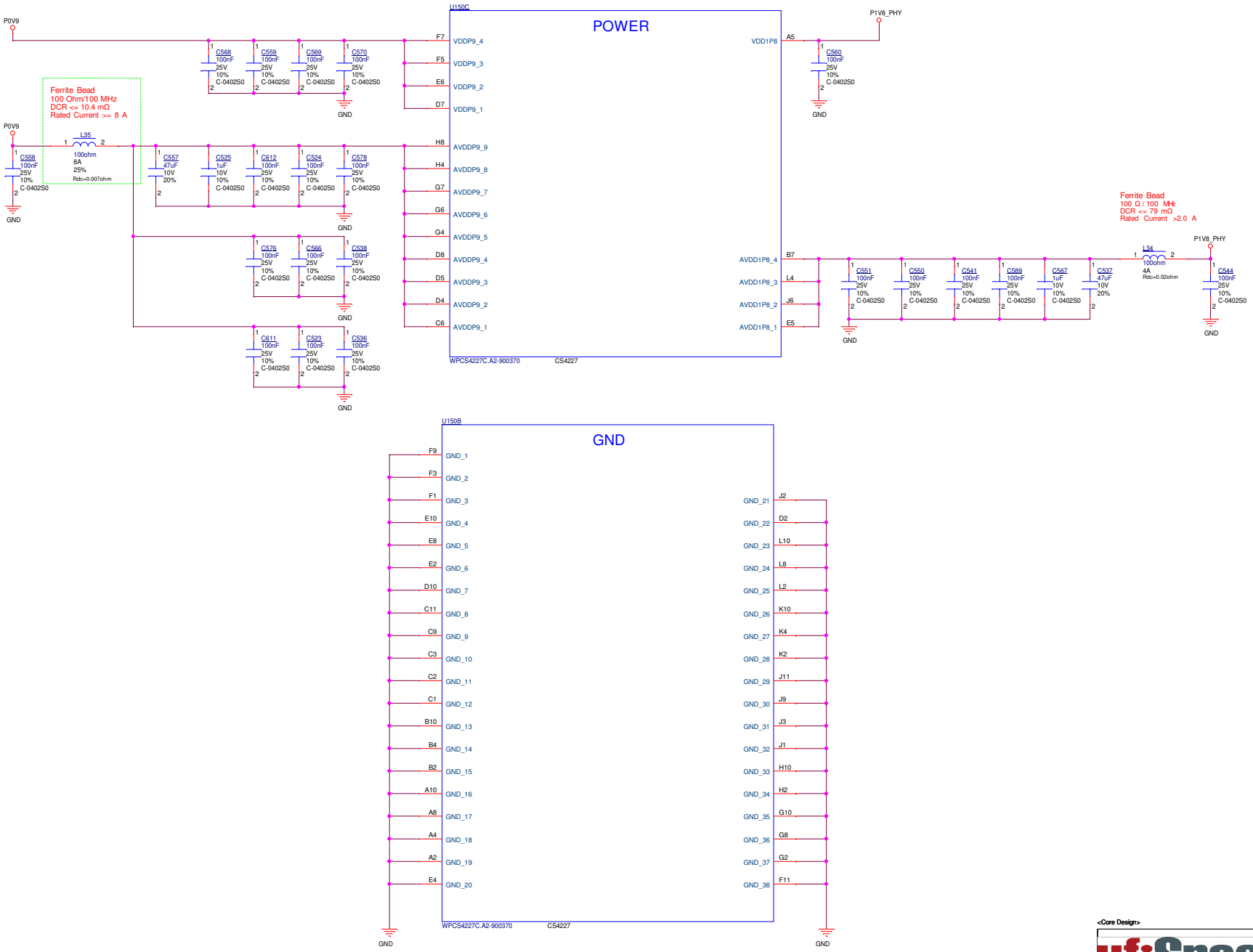
<Core Design>

UfiSpace Co., Ltd.

Title

095_CS4227_PHY

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	95 of 152	015



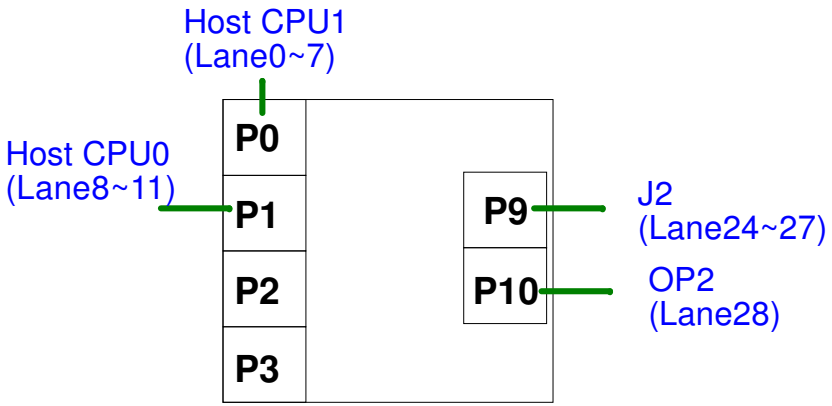
<Core Design>

UfiSpace Co., Ltd.

Title

096_CS4227_Power

Document Number: PCB P/N: T99O114T00	Sheet 96 of 152	Rev 015



U3A

PEX 8724

Station 0

PEX8724-CA80BC G

U3B

PEX 8724

Station 1

PEX8724-CA80BC G

<Variant Name>

UfiSpace Co., Ltd.

Title: 097_PCIE SW SerDes

Document Number: PCB P/N: T99O114T00

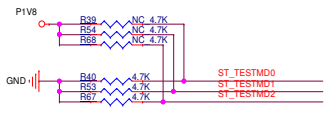
Sheet 97 of 152

Rev 015

ST_TESTKMD[2:0]

Config the I/O pin set, 0, 1, Z tri-state input

000 = Hot Plug A + Hot Plug C + Port Good[6:0]# + GPIO[10:7]

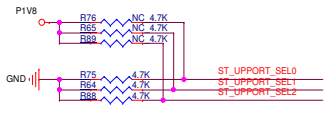


IP_UPPORT_SEL[2:0]

Base mode: select Up stream port
Virtual switch mode: select Management port

0, 1, Z tri-state input

000 = Port 0

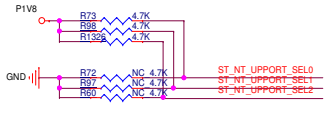


IP_NT_UPPORT_SEL[2:0]

Select Up stream NT port

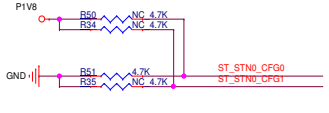
0, 1, Z tri-state input

111 = NT Port is disable



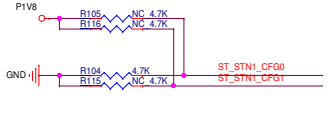
ST_STN0_CFG[1:0]

0Z = 1 = x16
01 = 2 = x8, x8
Z0 = 3 = x8, x4, x4
> ZZ = 4 = x4, x4, x4, x4



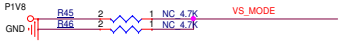
ST_STN1_CFG[1:0]

01 = 1 = x8
> Z0 = 2 = x4, x4



VS_MODE

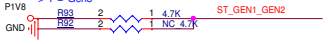
Number of virtual switch



ST_GEN1_GEN2

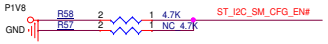
Select the max. speed of lens

0 = Gen 1
Z = Gen 2
> 1 = Gen3



ST_I2C_SM_CFG_EN#

0 = I2C/EEPROM initialize, set Initiate Configuration bit
> 1 = EEPROM initialize, donot set Initiate Configuration bit



ST_I2C_SM_EN

> 0 = Enable I2C slave protocol on I2C_SCL0/SDA0
Z = Enable SMBUS without ARP on I2C_SCL0/SDA0
1 = Enable SMBUS with ARP on I2C_SCL0/SDA0



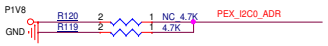
ST_MGMT_PEN

> 0 = Management port Enable, EEPROM initilaize, no clear and all link training
Z = Management port Enable, and only management port link training
1 = Management port disable



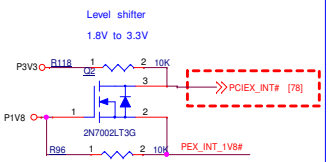
PEX_I2C0_ADR

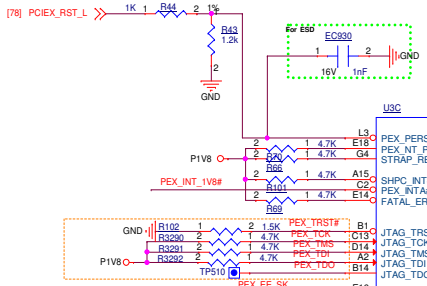
> 0 = 0b0111_000x
Z = 0b0111_001x
1 = 0b0111_010x

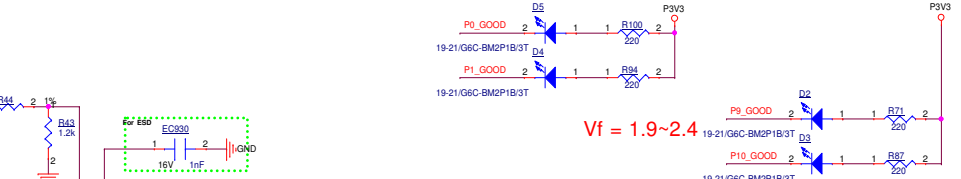


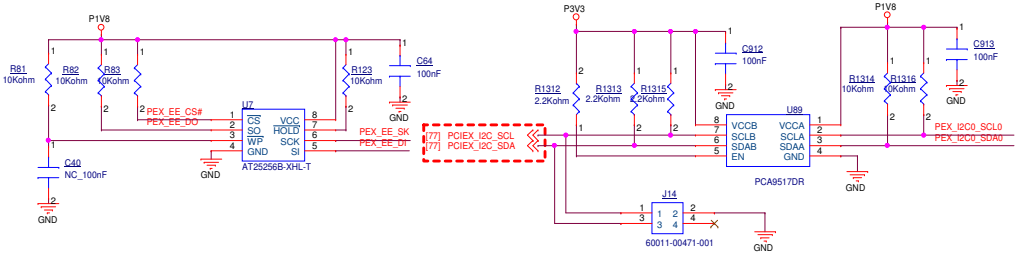
Level shifter

1.8V to 3.3V









<Variant Name>

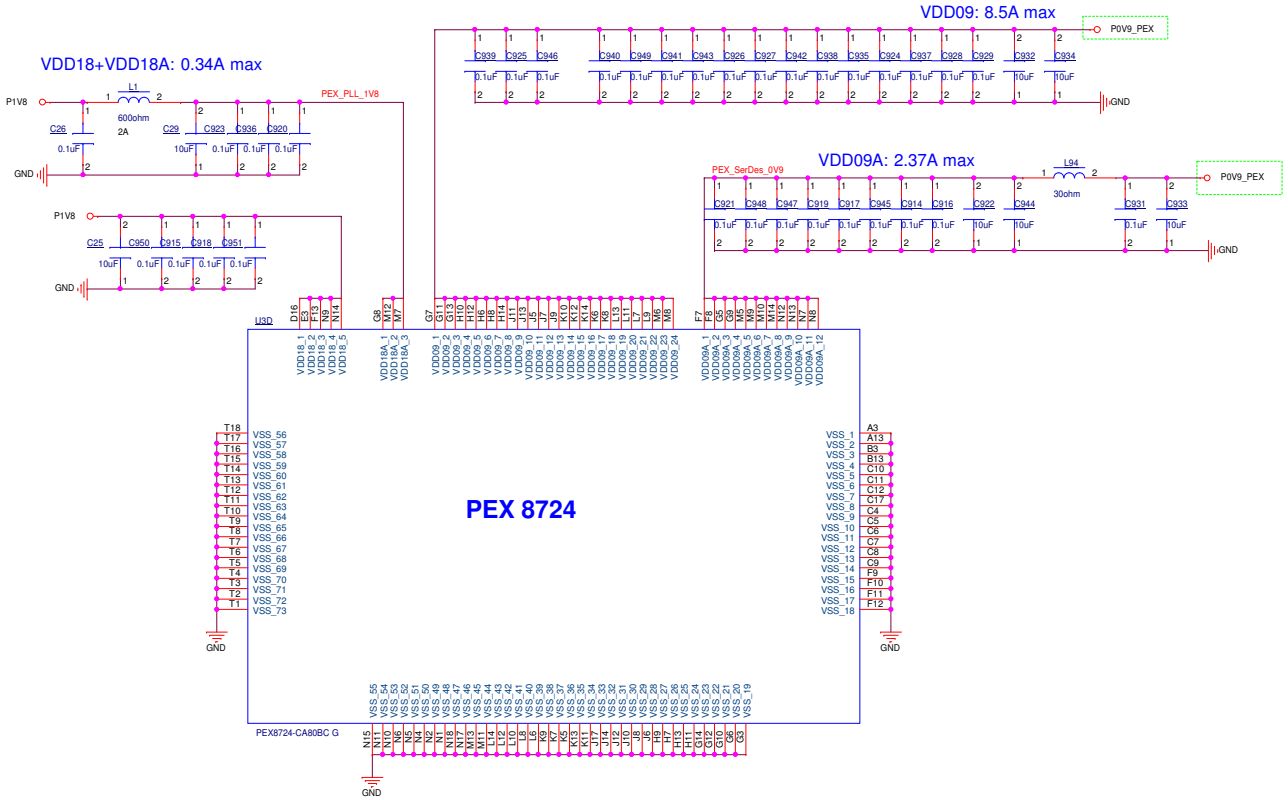
UfiSpace Co., Ltd.

Title: 098_PCIE SW MISC

Document Number: PCB P/N: T99O114T00

Sheet 98 of 152

Rev 015



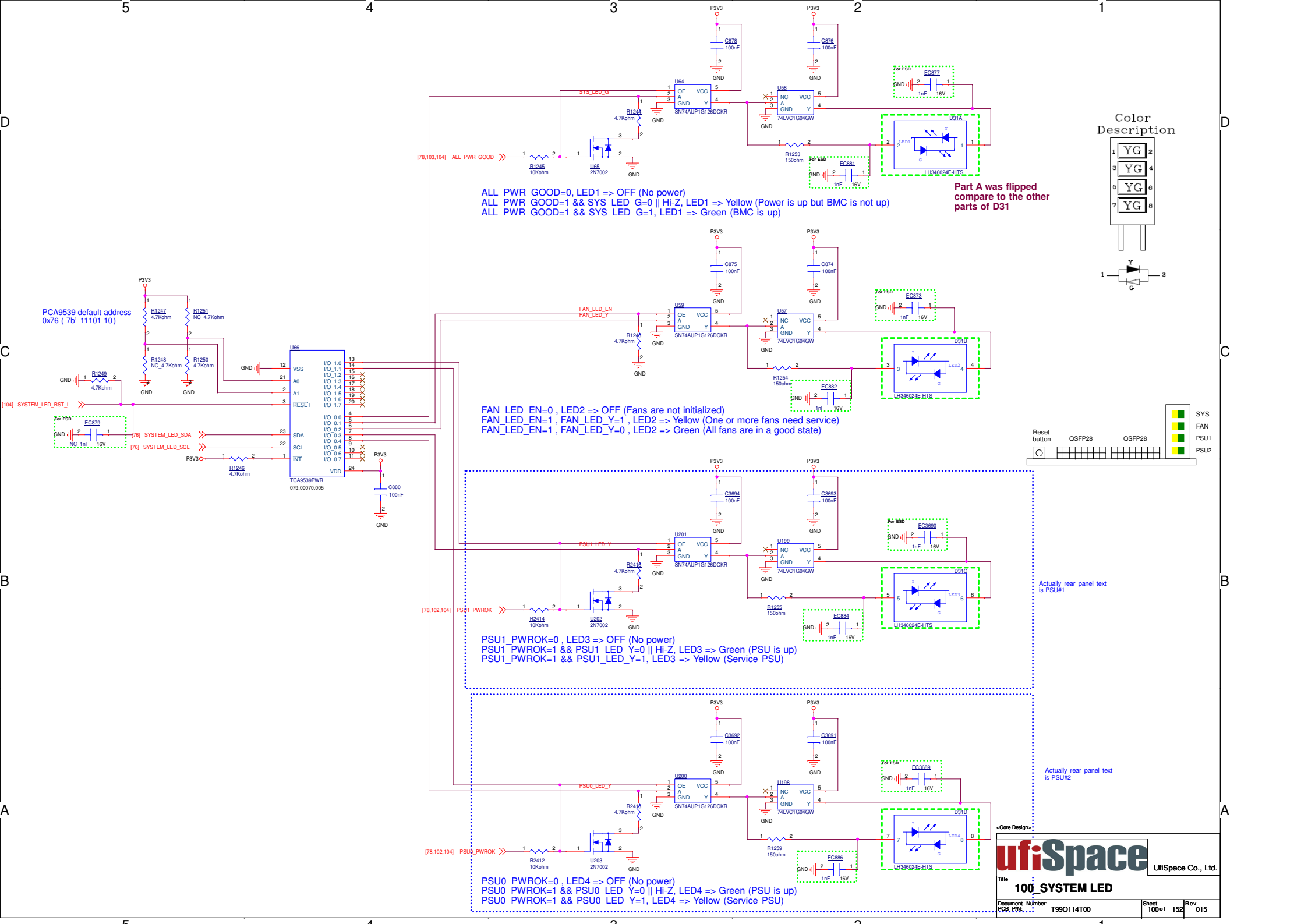
<variant_name>

UfiSpace Co., Ltd.

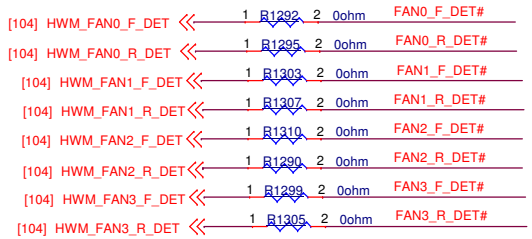
Title

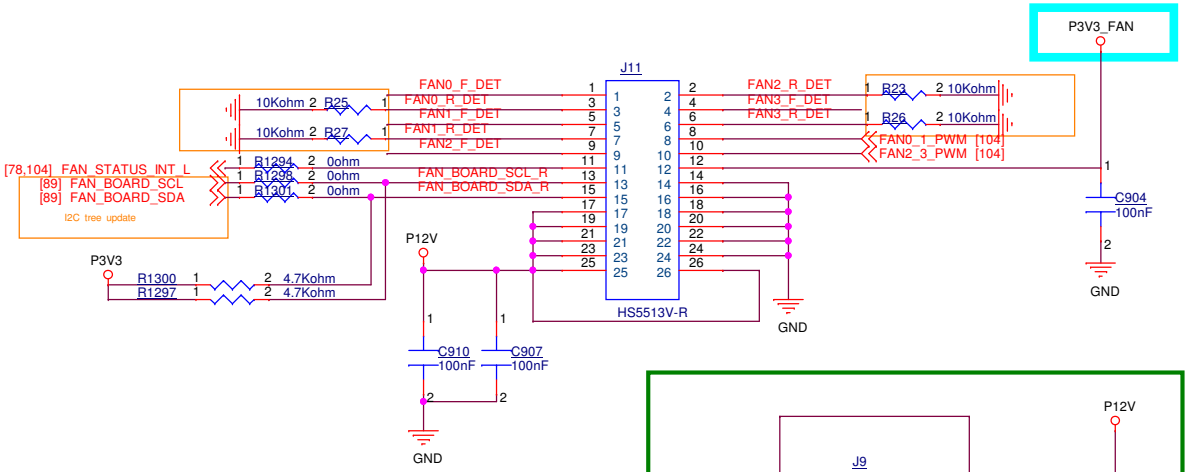
099_PCIE SW Power & GND

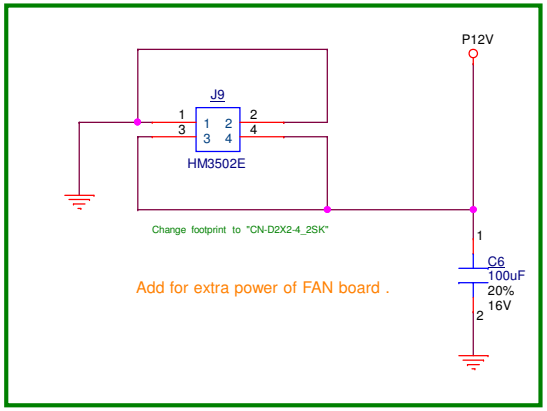
Document Number: PCB P/N: T99O114T00	Sheet 99 of 152	Rev 015

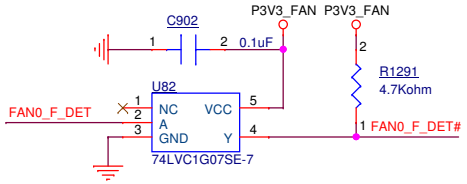

PCA9539 default address
0x76 (7b' 11101 10)
ALL_PWR_GOOD=0, LED1 => OFF (No power)
ALL_PWR_GOOD=1 && SYS_LED_G=0 || Hi-Z, LED1 => Yellow (Power is up but BMC is not up)
ALL_PWR_GOOD=1 && SYS_LED_G=1, LED1 => Green (BMC is up)
Part A was flipped compare to the other parts of D31
Color Description
FAN_LED_EN=0 , LED2 => OFF (Fans are not initialized)
FAN_LED_EN=1 , FAN_LED_Y=1 , LED2 => Yellow (One or more fans need service)
FAN_LED_EN=1 , FAN_LED_Y=0 , LED2 => Green (All fans are in a good state)
Reset button
QSFP28
QSFP28
SYS
FAN
PSU1
PSU2
PSU1_PWROK=0 , LED3 => OFF (No power)
PSU1_PWROK=1 && PSU1_LED_Y=0 || Hi-Z, LED3 => Green (PSU is up)
PSU1_PWROK=1 && PSU1_LED_Y=1, LED3 => Yellow (Service PSU)
Actually rear panel text is PSU#1
PSU0_PWROK=0 , LED4 => OFF (No power)
PSU0_PWROK=1 && PSU0_LED_Y=0 || Hi-Z, LED4 => Green (PSU is up)
PSU0_PWROK=1 && PSU0_LED_Y=1, LED4 => Yellow (Service PSU)
Actually rear panel text is PSU#2
<Core Design>
UfiSpace Co., Ltd.
Title
100_SYSTEM LED
Document Number:
PCB P/N: T99O114T00
Sheet 100 of 152
Rev 015

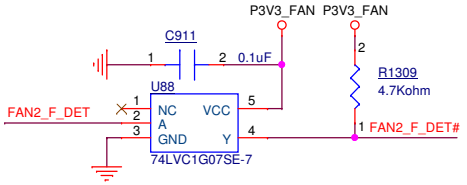
TO FAN BOARD CONNECTOR

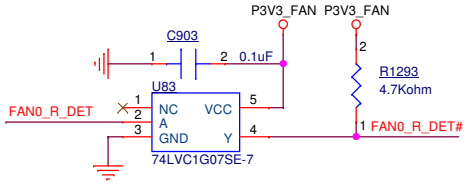


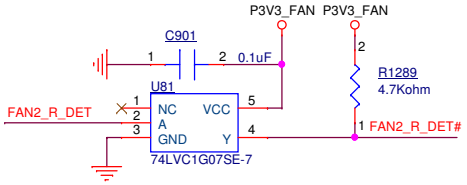


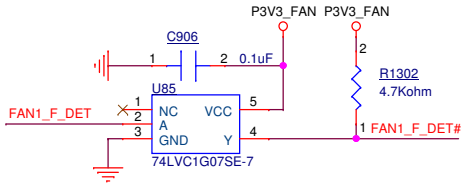


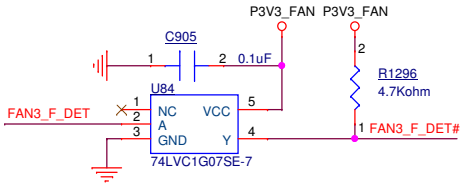


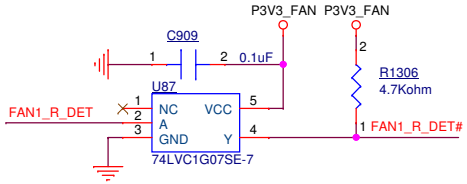


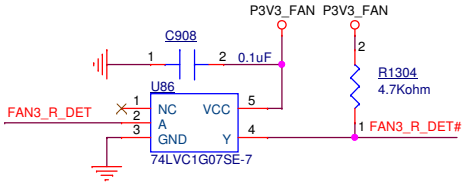












<Core Design>

UfiSpace Co., Ltd.

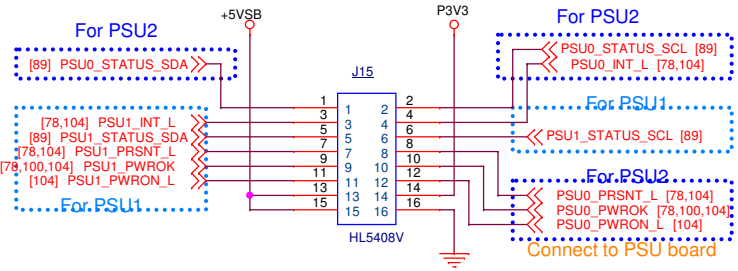
Title
101_FAN CONNECTOR

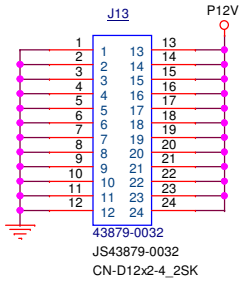
Document Number: PCB P/N:	Sheet	Rev
T99O114T00	101 of 152	015

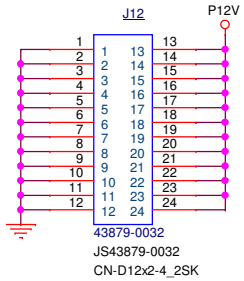
POWER CONNECTOR

PSU CONNECTOR 0 (LEFT)
I2C ADDRESS 0x1010000X

PSU CONNECTOR 1 (RIGHT)
I2C ADDRESS 0x1010000X





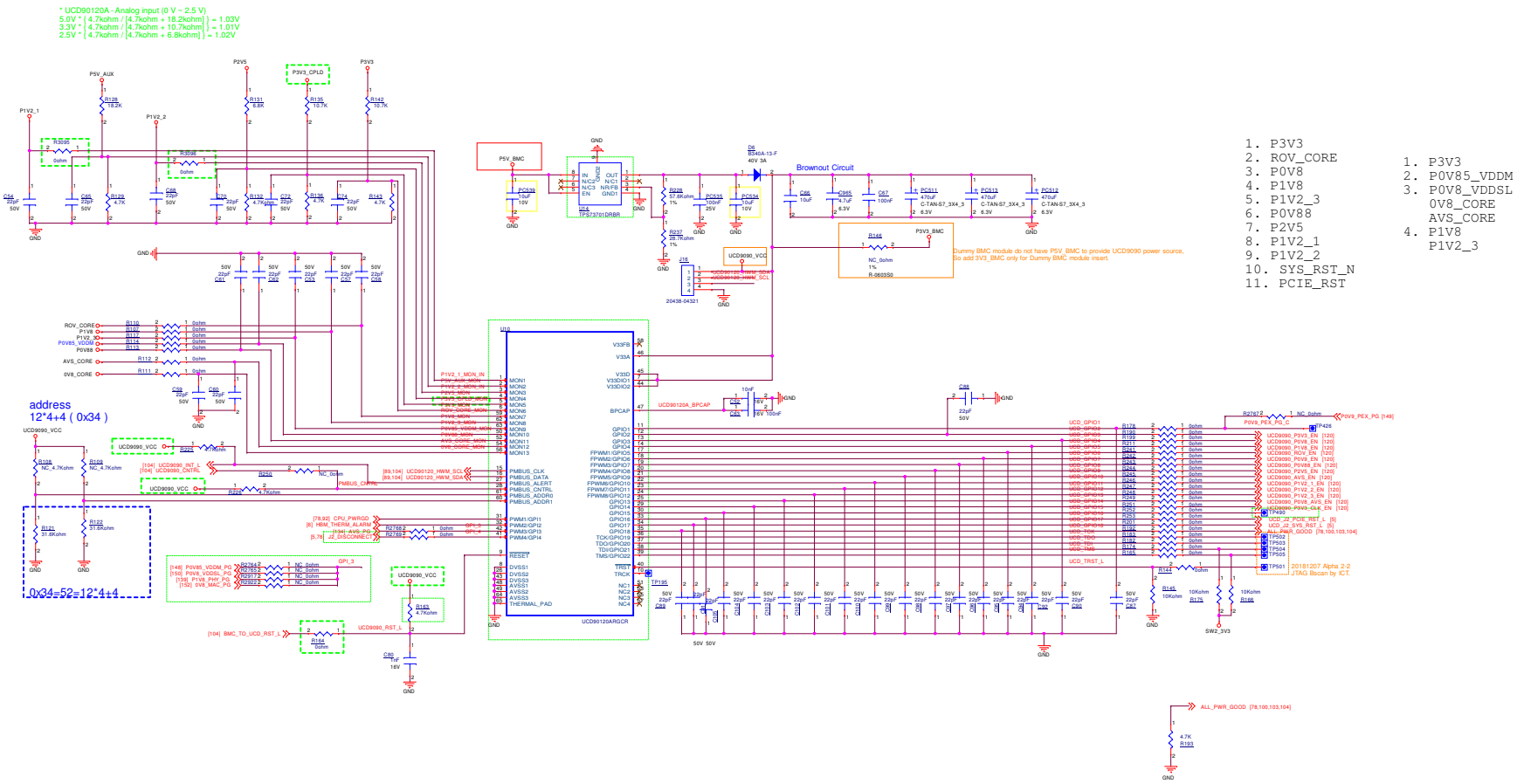


<Core Design>

UfiSpace Co., Ltd.

Title
102_POWER CONNECTOR

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	102 of 152	015

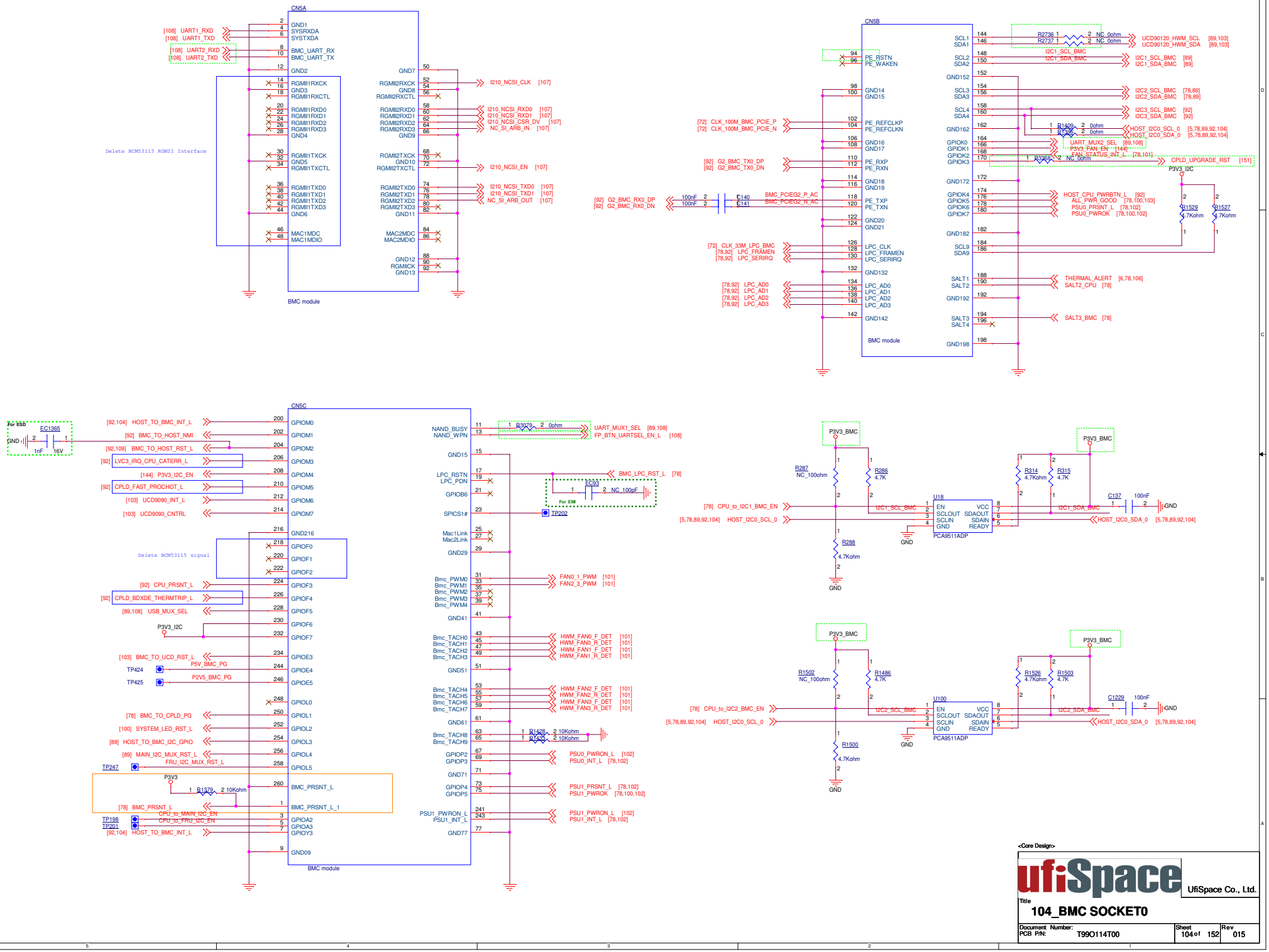


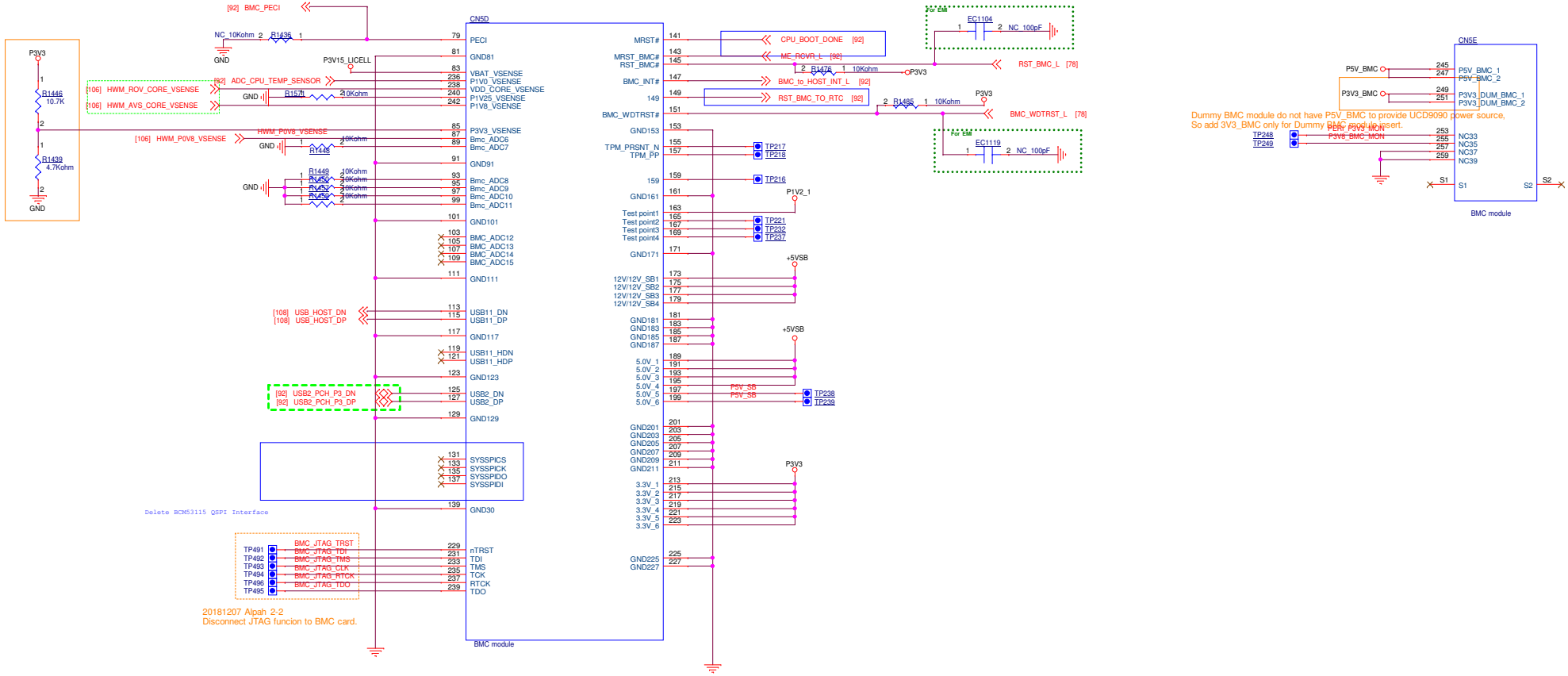
1. P3V3
2. ROV_CORE
3. P0V8
4. P1V8
5. P1V2_3
6. P0V88
7. P2V5
8. P1V2_1
9. P1V2_2
10. SYS_RST_N
11. PCIE_RST

1. P3V3
2. P0V85_VDDM
3. P0V8_VDDSL
   0V8_CORE
   AVS_CORE
4. P1V8
   P1V2_3

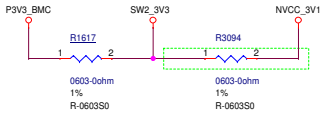
<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title: 103_UCD90120A			
Document Number: PCB P/N: T99O114T00	Sheet 103 of 152	Rev 015	

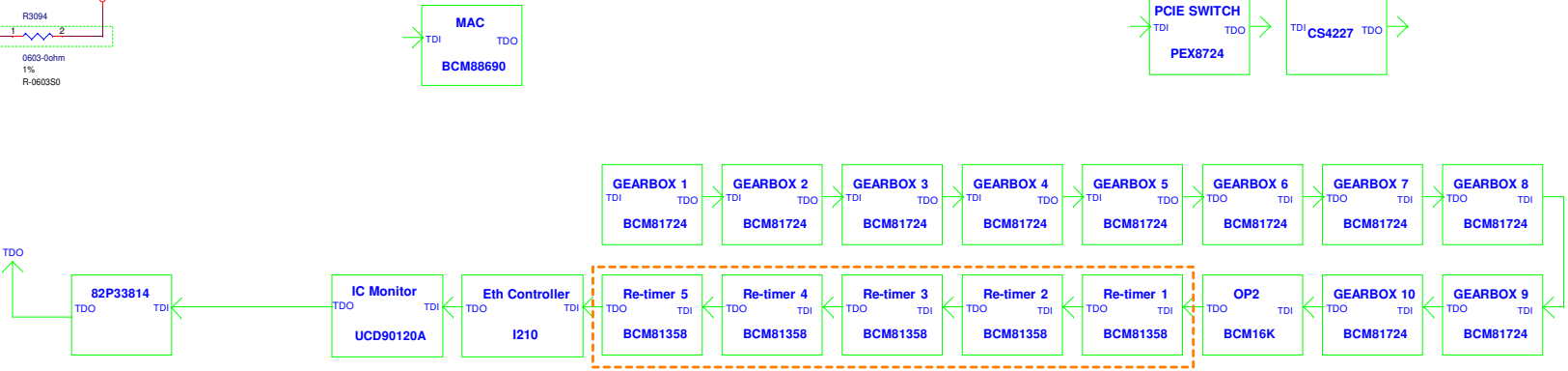

CN5A
BMC module
Delete BCM53115 RGMII Interface
CN5B
BMC module
CN5C
BMC module
Delete BCM53115 signal
UFISPACE
Core Design
UfiSpace Co., Ltd.
Title
104_BMC SOCKET0
Document Number:
PCB P/N:
T99O114T00
Sheet
104 of 152
Rev
015



SW Note:
Default power-up voltage of SW2_3V3 is 3.3V.
Need to change it to 3.1V after boot-up
to lower power consumption.



BOUNDARY SCAN
TEST POINTS

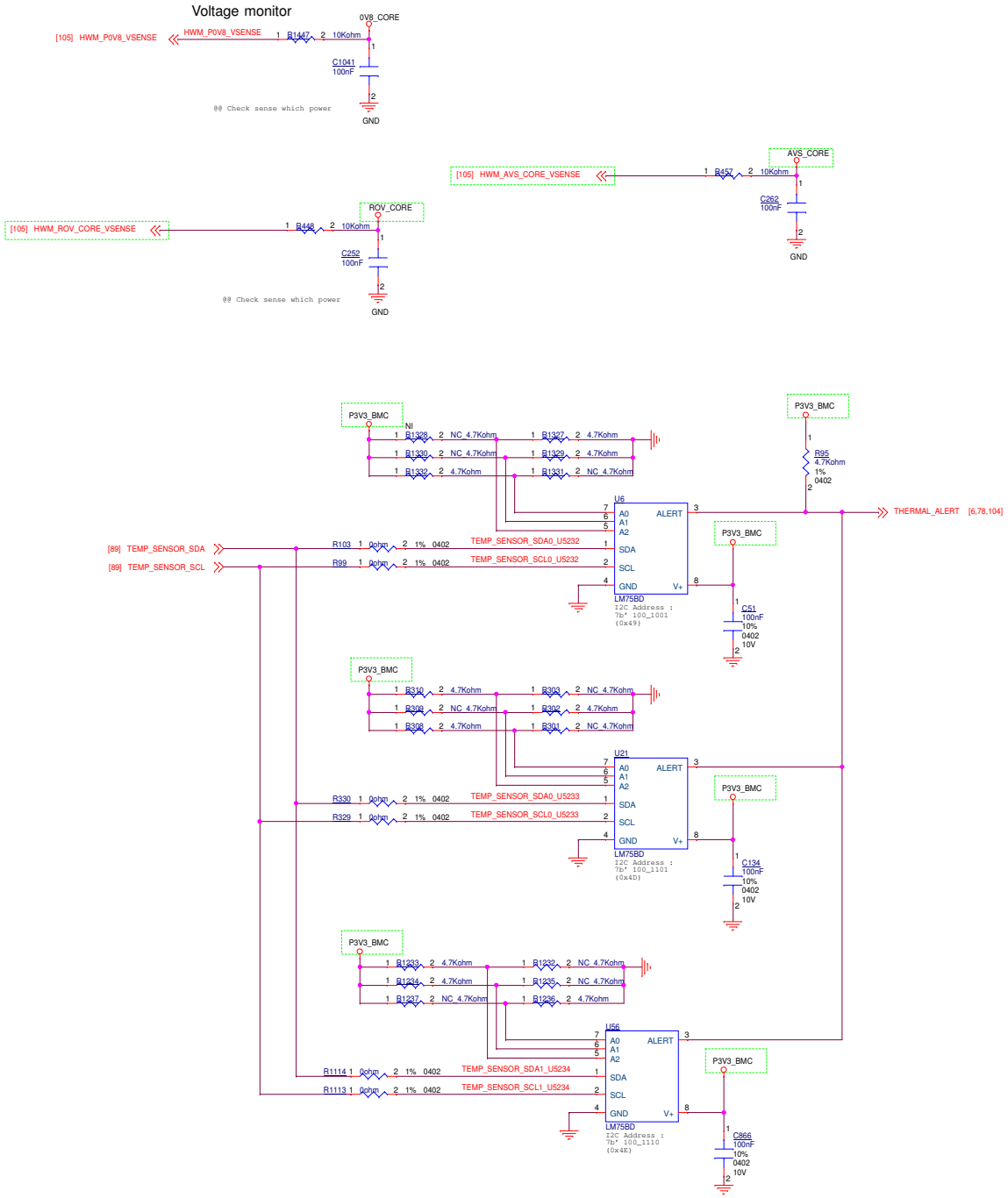


<Core Design>

UfiSpace Co., Ltd.

Title
105_BMC SOCKET1

Document Number:		Sheet	Rev
PCB P/N: T99O114T00		105 of 152	015



LM75BD replace thermal resistor for better thermal accurancy

<Core Design>

UfiSpace Co., Ltd.

Title: 106_HWM

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	106 of 152	015

Refers to "475120_I210_I211_Design_Guide_rev_1_5", p-10
I210 supports a 1MHz SMBus

NOTE: Default SMBus Address is 0xC2

Add NCSI interface connection to BMC module

To OOB Board Connector

Place SO series term (R5653) near the flash U5185

NVM 16Mb

Use for EEPROM code programming.

Based on checklist rev2.1: If a Flash is not used add a 3.3Kohm pull-up to NVM_SO

Disable security and the iNVM LOCK by pulling down NVM_SI during power up.

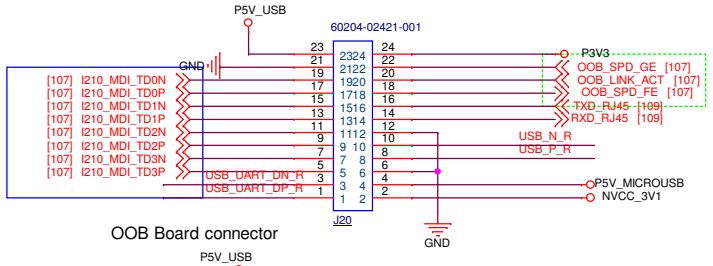
<Core Design>

UfiSpace Co., Ltd.

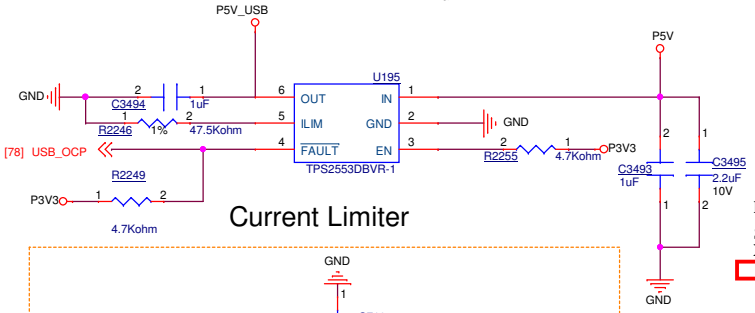
Title: 107_ETH CONTROLLER WGI210AT

Document Number: PCB P/N: T99O114T00 | Sheet 107 of 152 | Rev 015

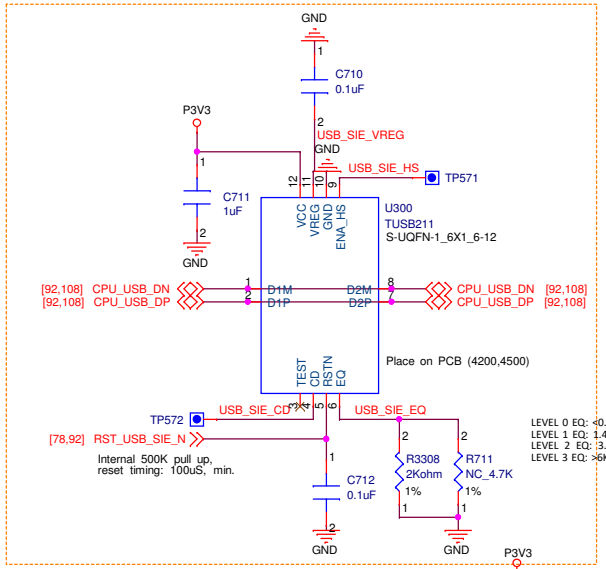
OOB PORT RJ-45 + Console Connector



OOB Board connector



Current Limiter

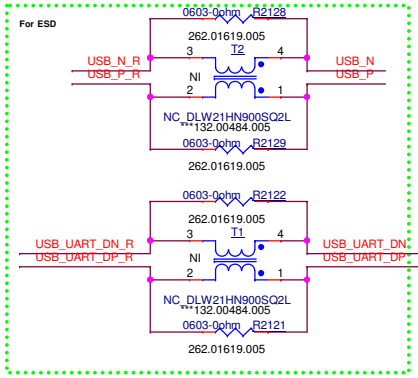


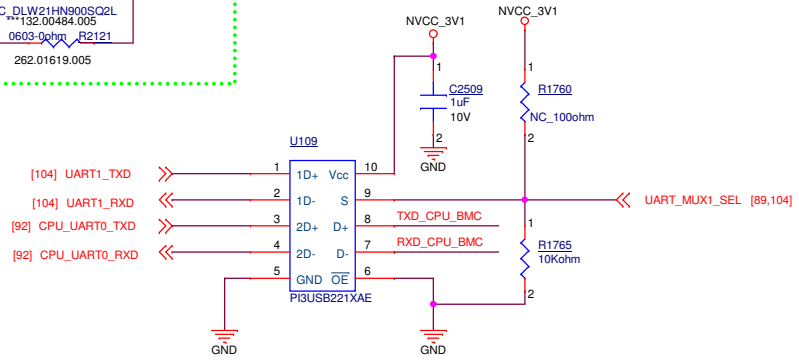
Default :

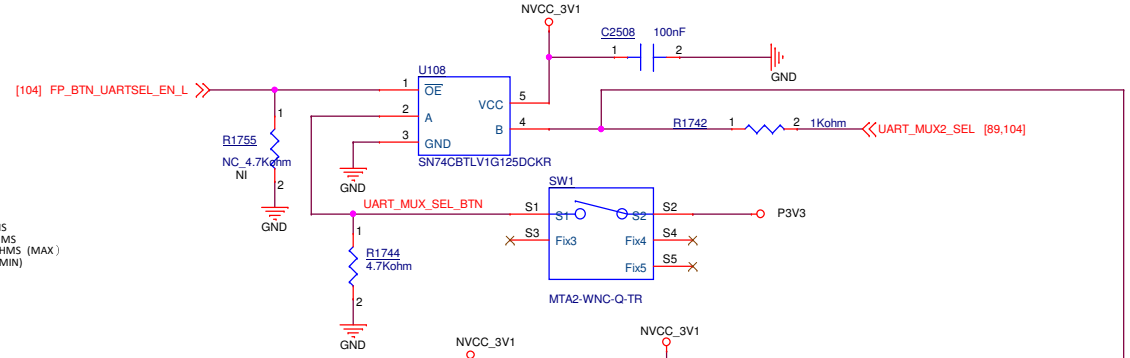
S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

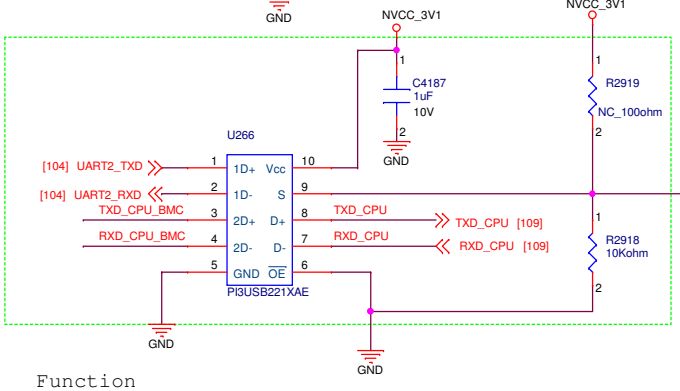
EN : Active High

Select R(Limit) = 47.5K ohm
Current Limit (max) = 22980V/47.5K^0.94 = 610mA
Current Limit (min) = 25230V/47.5K^1.016 = 500mA

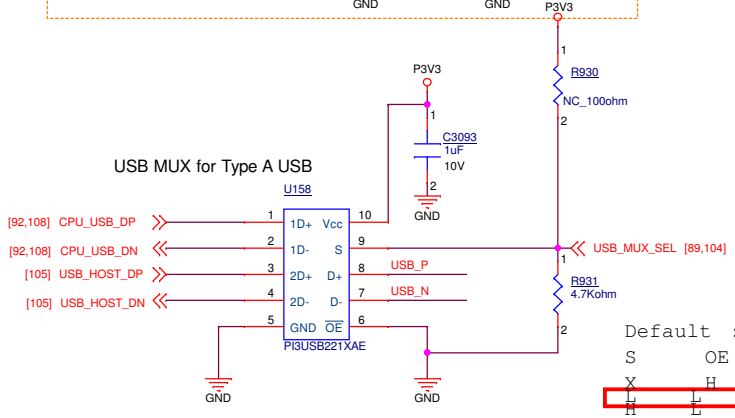








USB MUX for Type A USB



Default :

S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

<Core Design>

UfiSpace Co., Ltd.

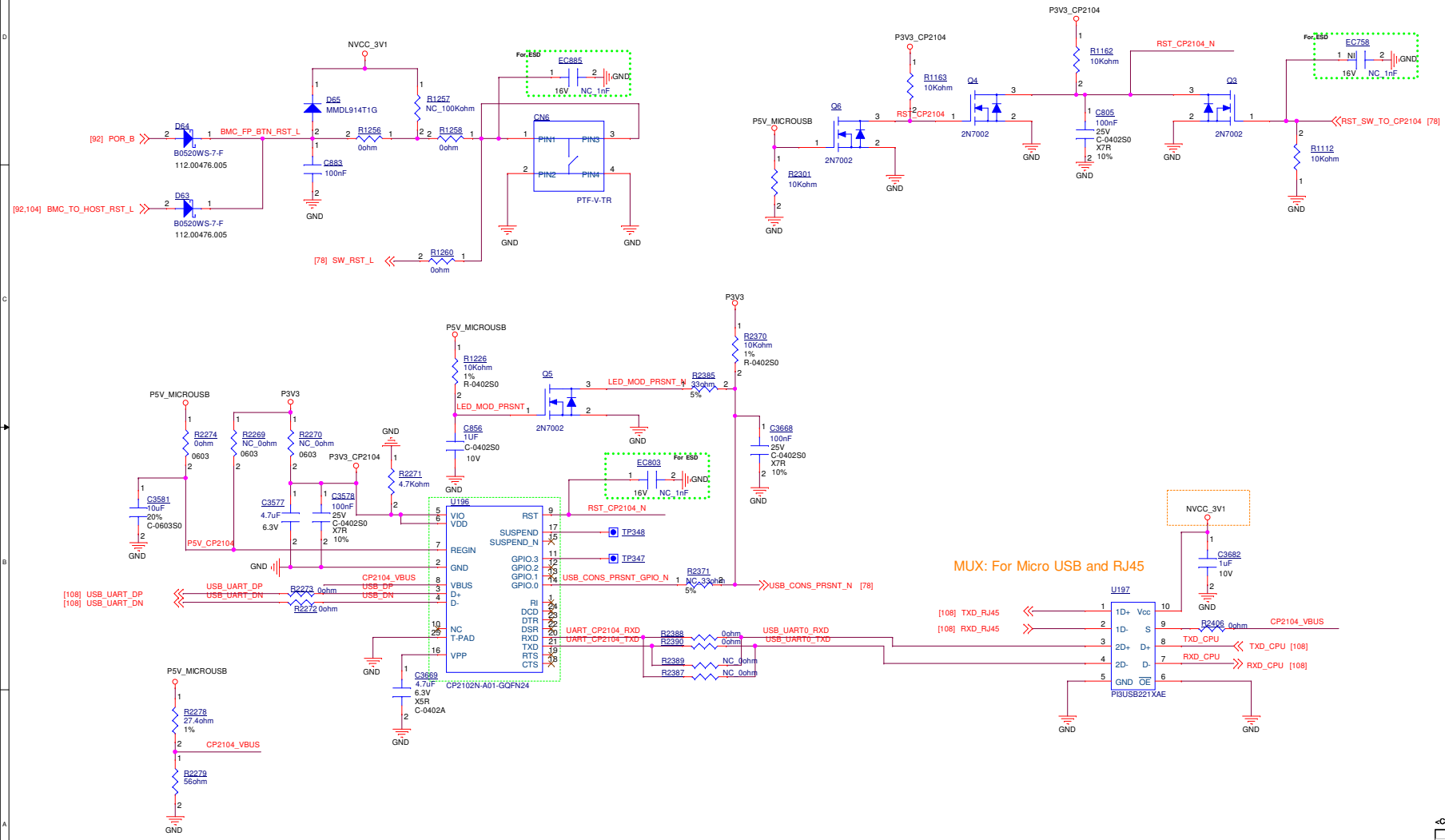
Title: 108_CONSOLE & OOB & USB

Document Number: PCB P/N: T99O114T00

Sheet 108 of 152

Rev 015

PUSH BUTTON & MICRO USB



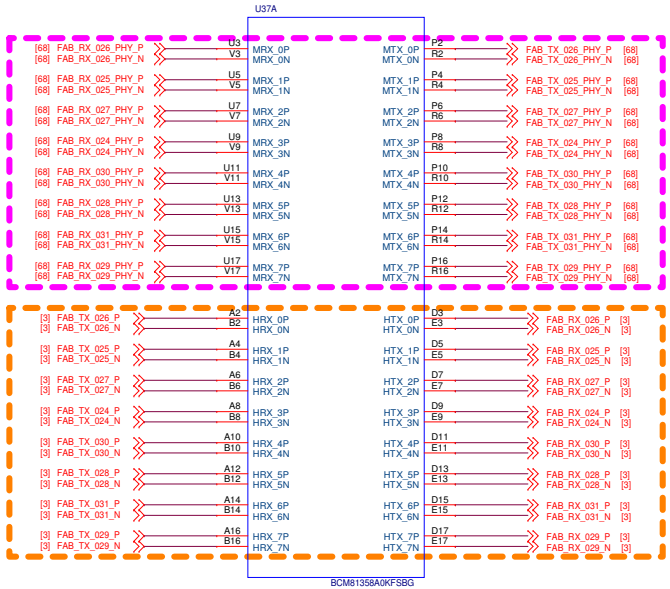
<Core Design>

UfiSpace Co., Ltd.

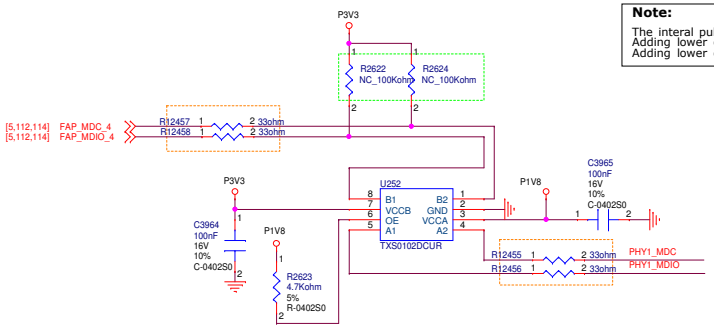
Title: 109_PUSH BUTTON &MICRO USB

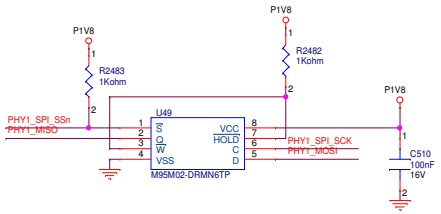
Document PCB P/N:	Number:	Sheet	Rev
	T99O114T00	109 of 152	015

Re-timer To QSFP-DD



MAC To Re-timer





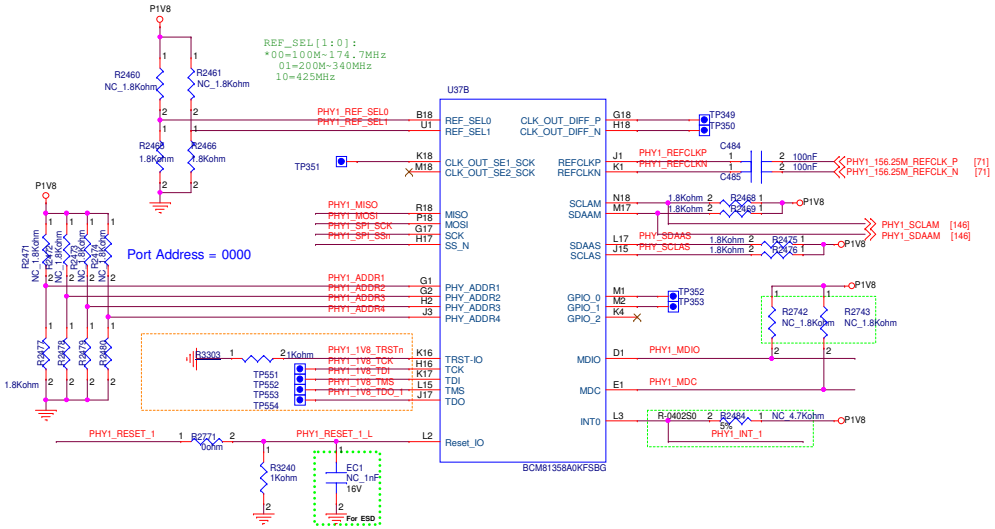
6.3 Recommended Operating Conditions

V_{SS} is the supply voltage associated with the input port; V_{SSO} is the supply voltage associated with the output port.

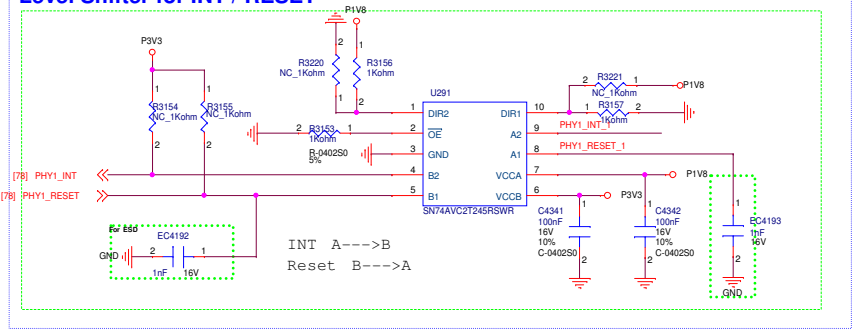
		MIN	MAX	UNIT
V_{DDA} Supply voltage[1]		1.65	3.6	V
V_{DDB} Supply voltage		2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.



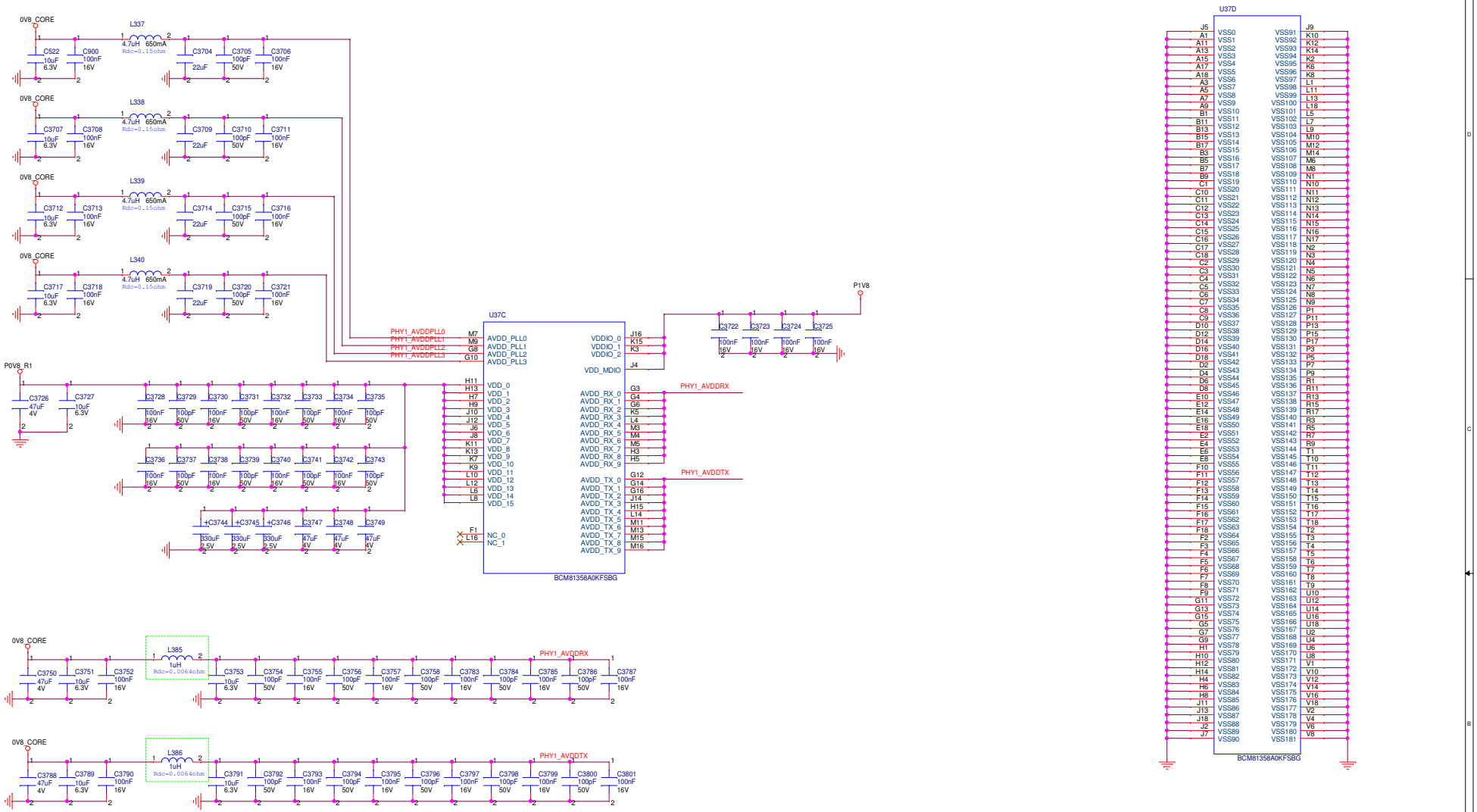
Level Shifter for INT / RESET



<Core Design>
UfiSpace Co., Ltd.

Title: 110_BCM81358_PHY1_A

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	110 of 152	015



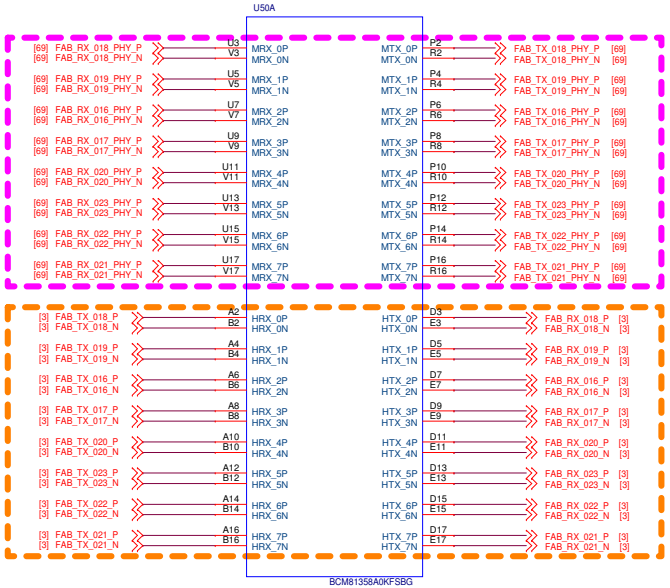
<Core Design>

UfiSpace Co., Ltd.

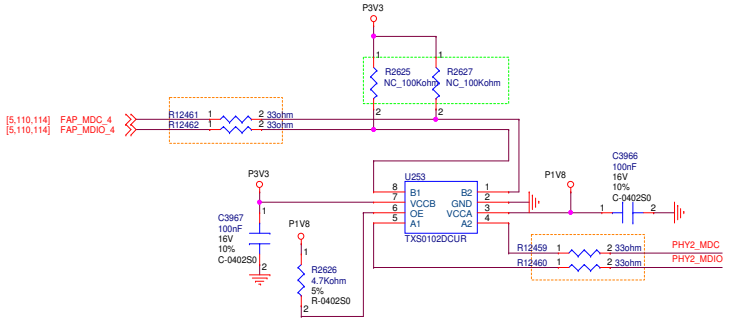
Title: 111_BCM81358_PHY1_B

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	111 of 152	015

Re-timer To QSFP-DD



MAC To Re-timer



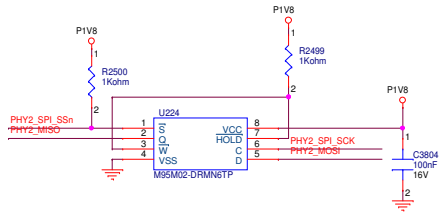
6.3 Recommended Operating Conditions

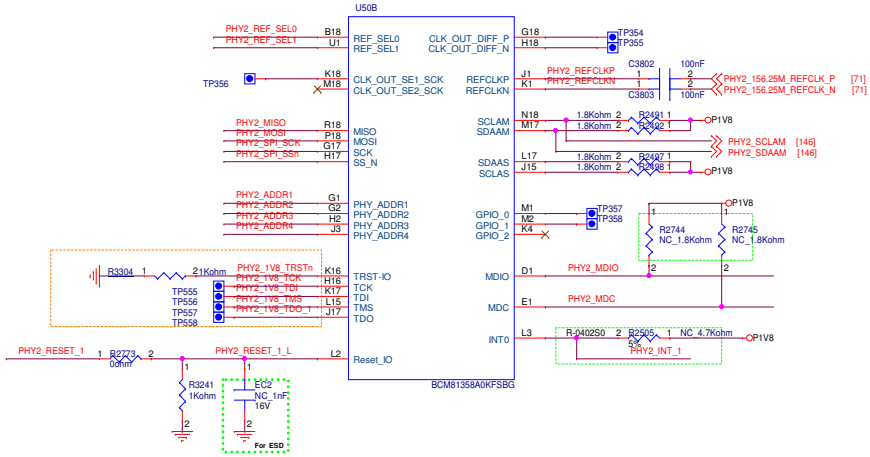
V_{DD} is the supply voltage associated with the input port. V_{DDO} is the supply voltage associated with the output port.

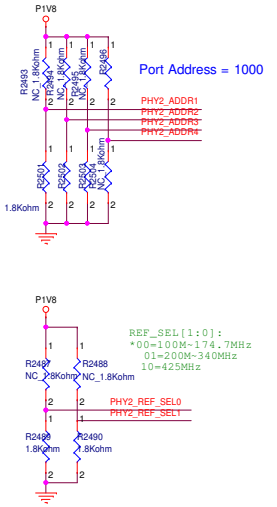
		MIN	MAX	UNIT
V_{DDA}	Supply voltage[1]	1.65	3.6	V
V_{DDB}	Supply voltage	2.3	5.5	V

Note:

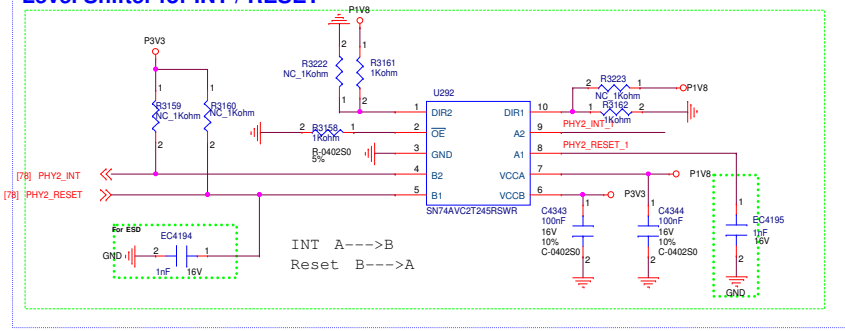
The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.







Level Shifter for INT / RESET

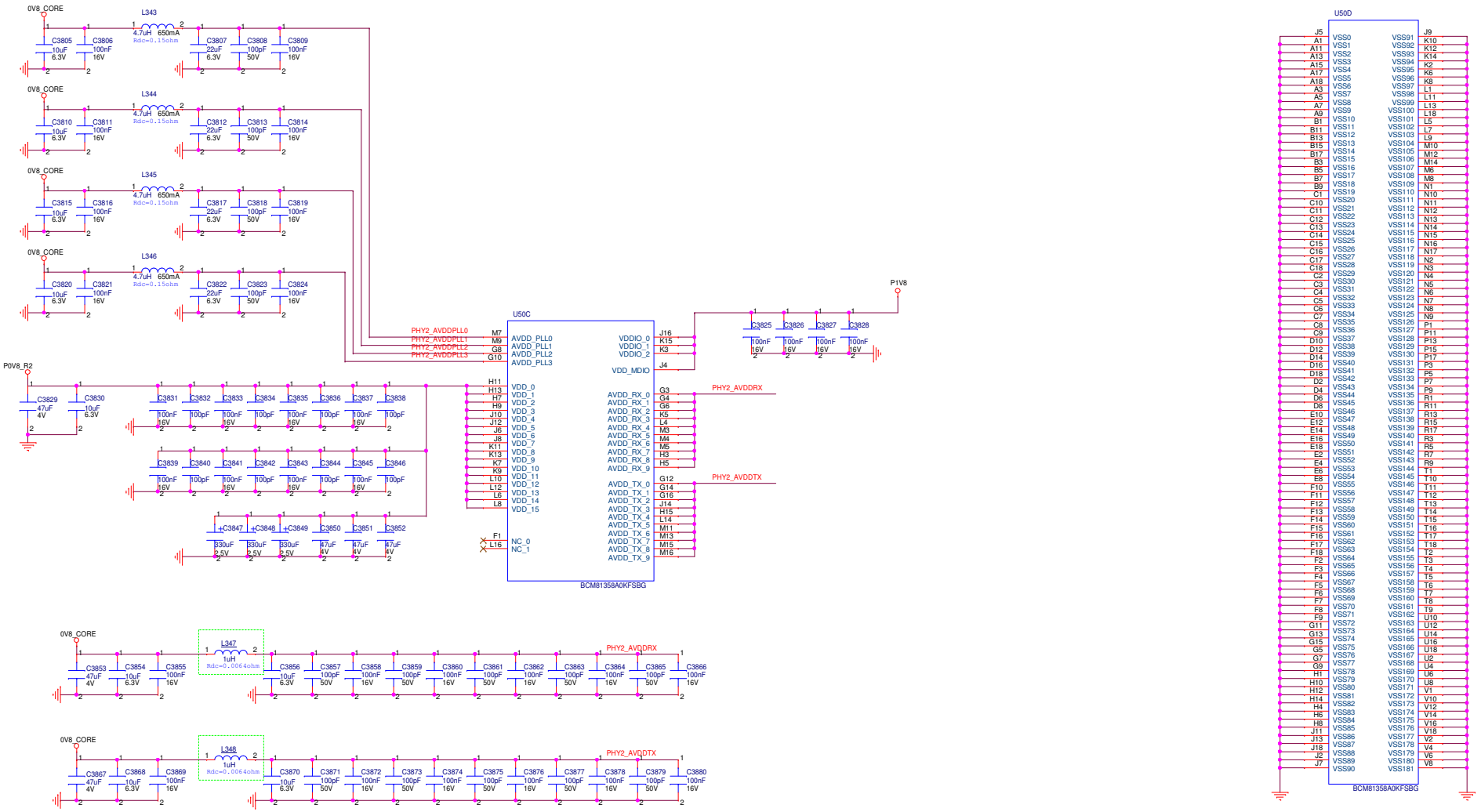


<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title: 112_BCM81358_PHY2_A

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	112 of 152	015



<Core Design>

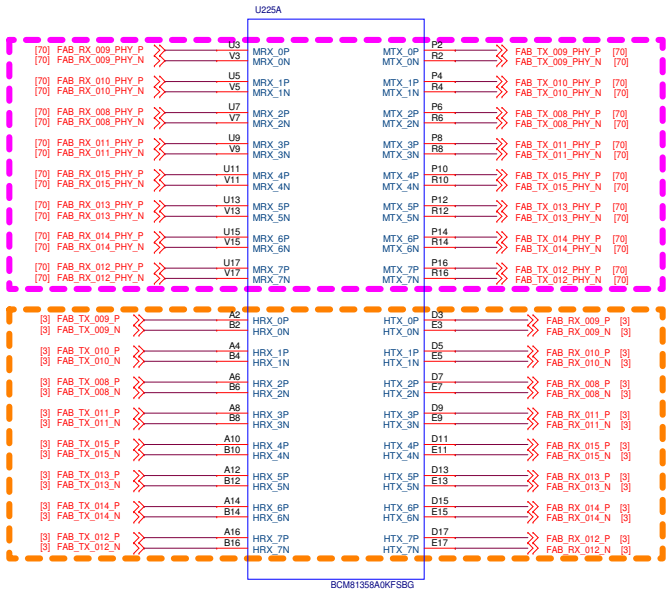
UfiSpace Co., Ltd.

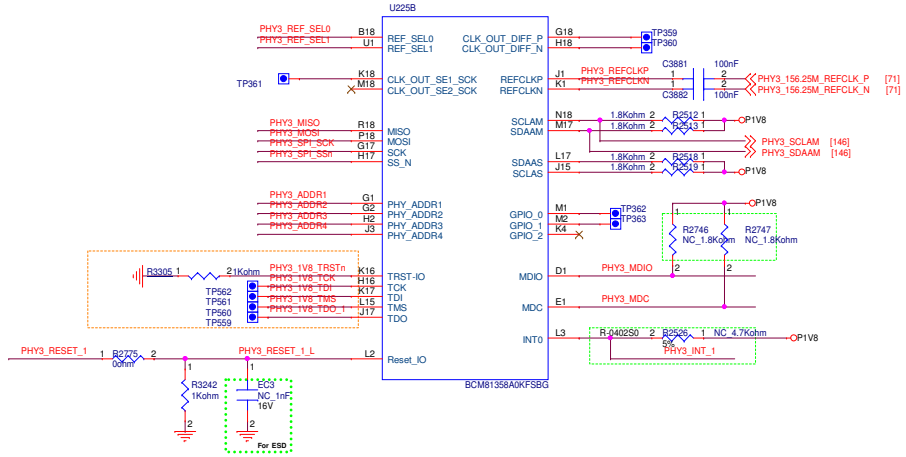
Title

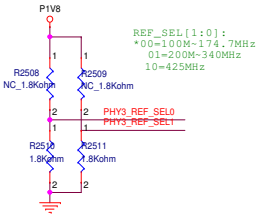
113_BCM81358_PHY2_B

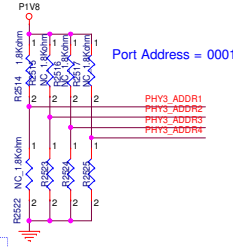
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	113 of 152	015

Re-timer To QSFP-DD

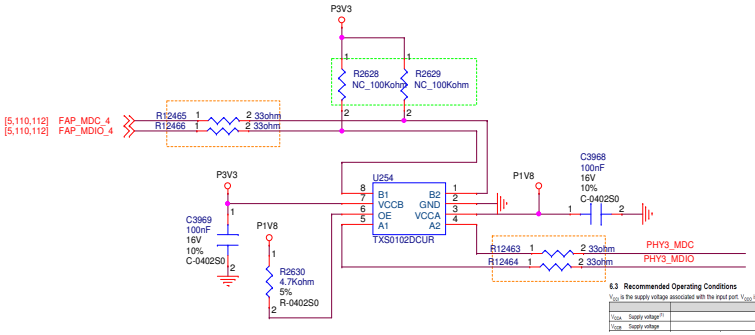








MAC To Re-timer

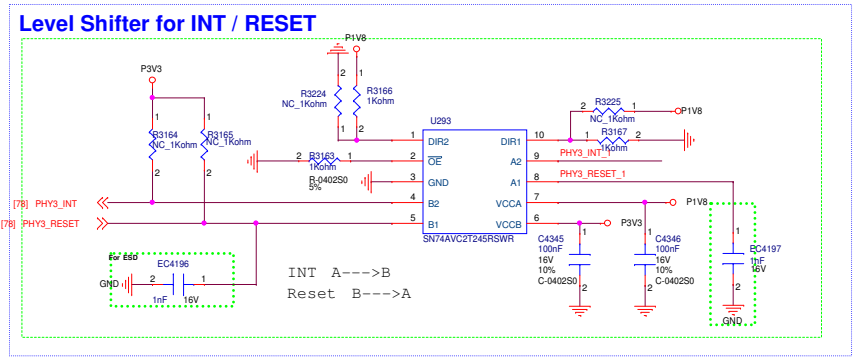


6.3 Recommended Operating Conditions

V_{CCA} is the supply voltage associated with the input port. V_{CCB} is the supply voltage associated with the output port.

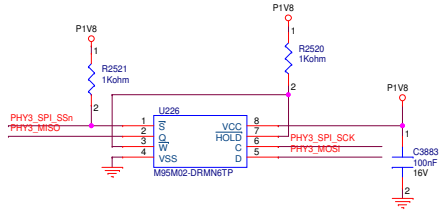
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

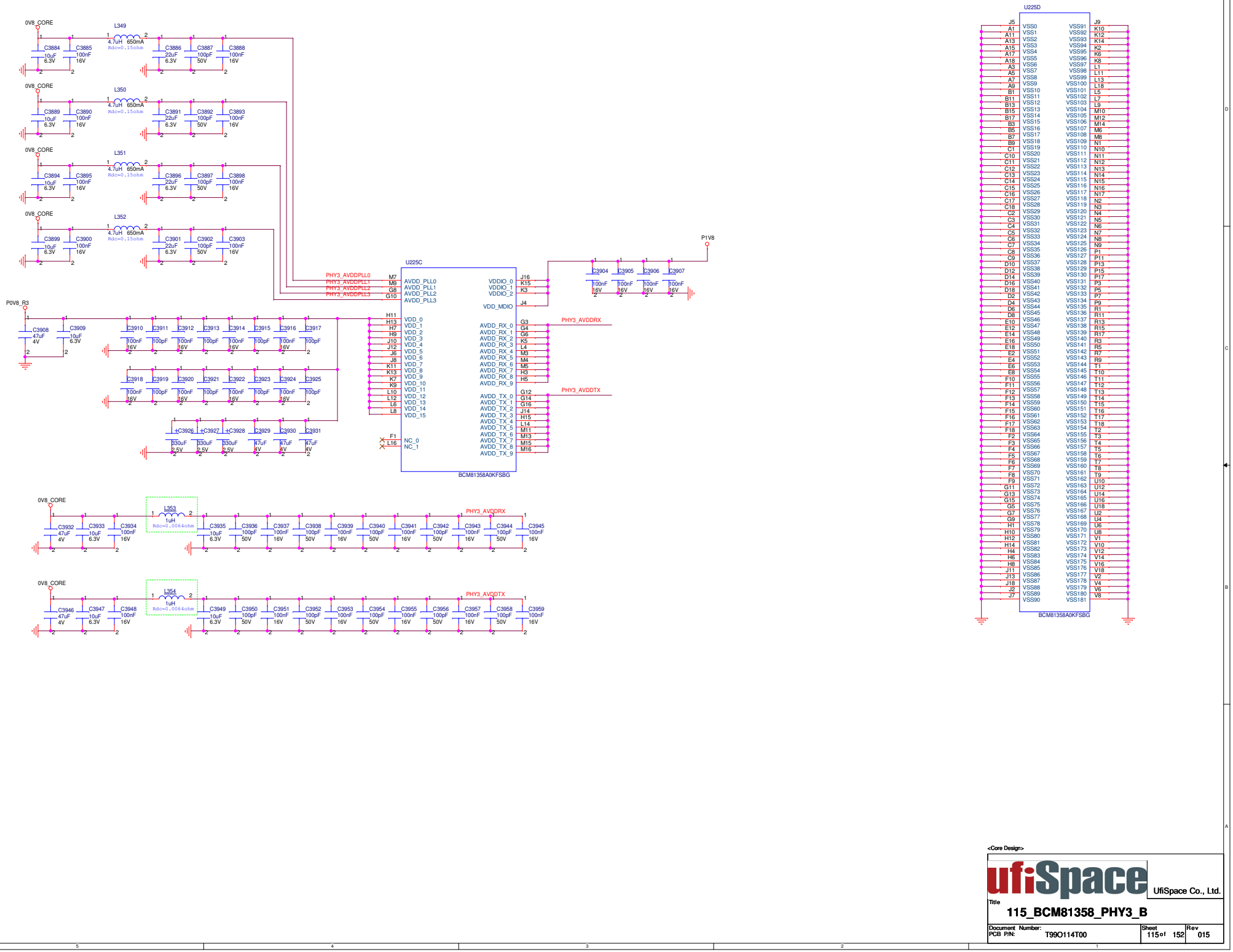
Level Shifter for INT / RESET



Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.





<Core Design>

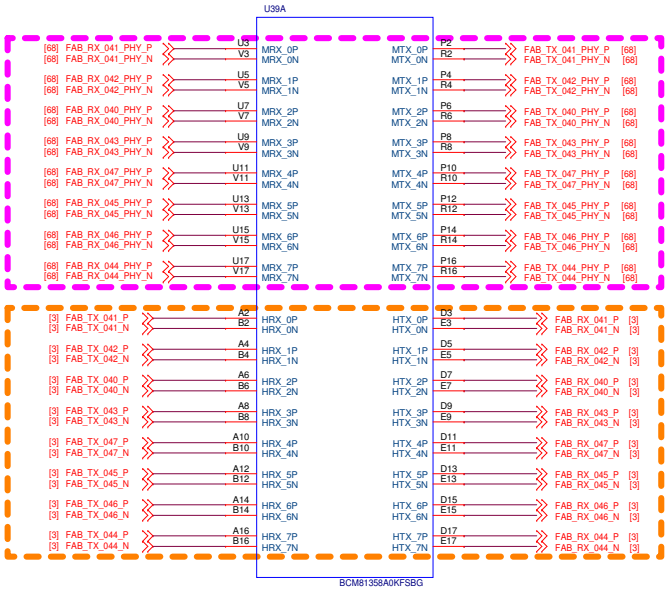
UfiSpace Co., Ltd.

Title

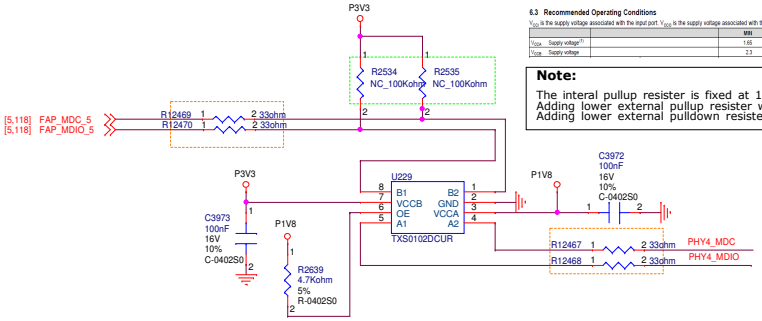
115_BCM81358_PHY3_B

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	115 of 152	015

Re-timer To QSFP-DD



MAC To Re-timer



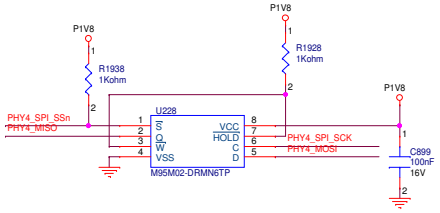
6.3 Recommended Operating Conditions

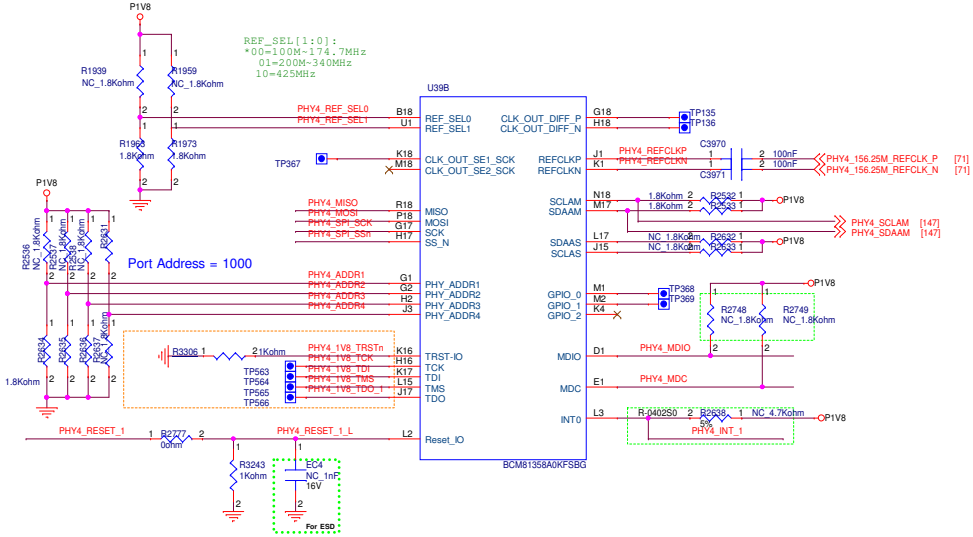
V_{IO} is the supply voltage associated with the input port. V_{OS} is the supply voltage associated with the output port.

		MIN	MAX	UNIT
V_{IOA} Supply voltage[1]		1.65	3.6	V
V_{IOB} Supply voltage		2.3	5.5	V

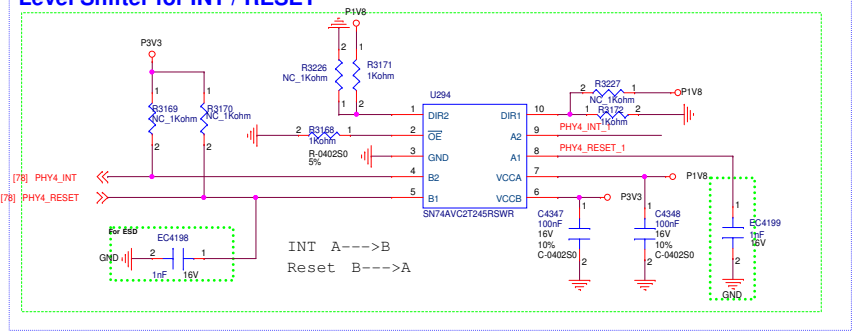
Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.





Level Shifter for INT / RESET

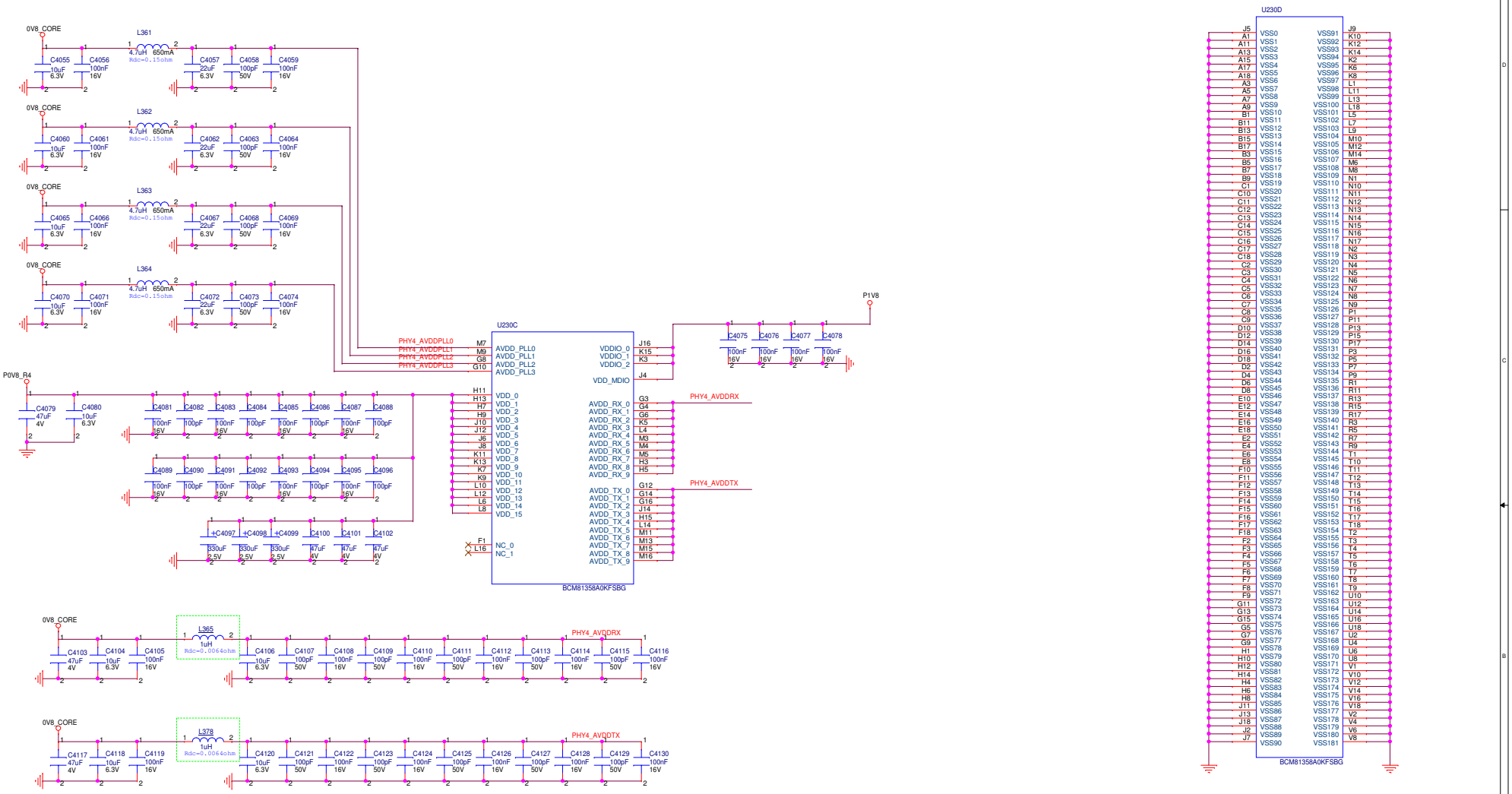


<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title: 116_BCM81358_PHY4_A

Document Number: PCB P/N: T99O114T00	Sheet 116 of 152	Rev 015



<Core Design>

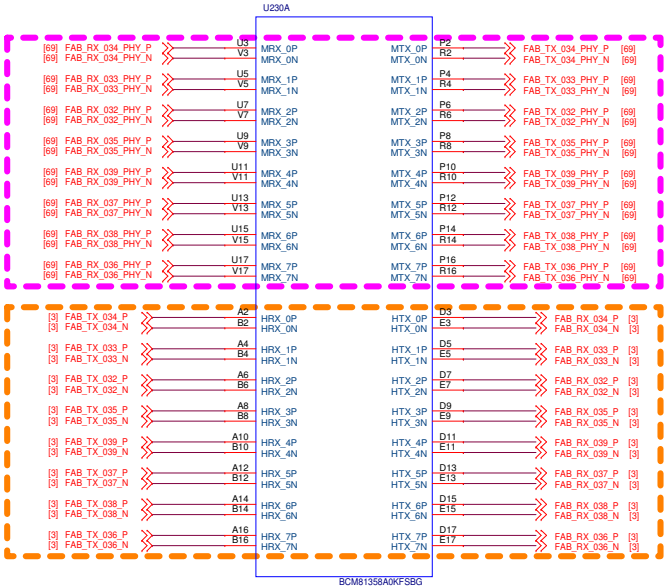
UfiSpace Co., Ltd.

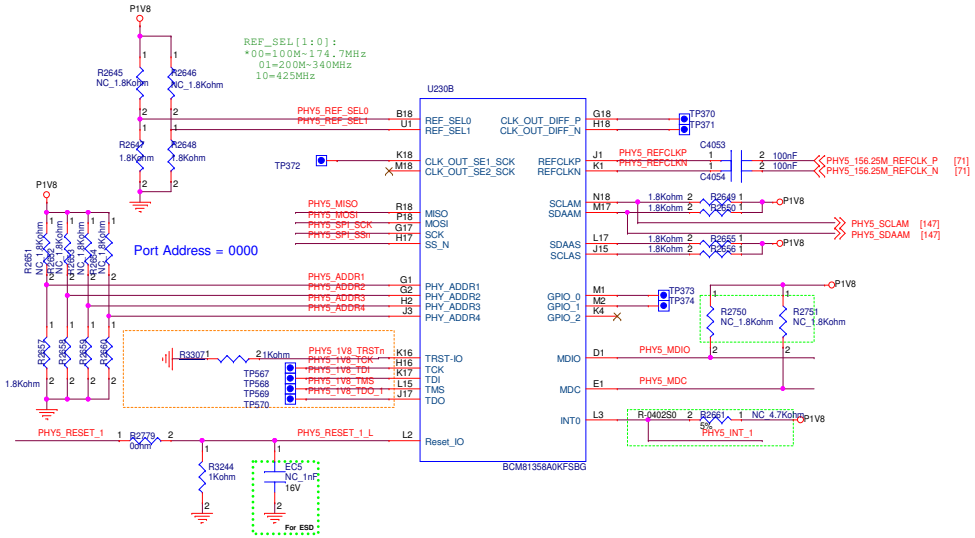
Title

117_BCM81358_PHY4_B

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	117 of 152	015

Re-timer To QSFP-DD





MAC To Re-timer

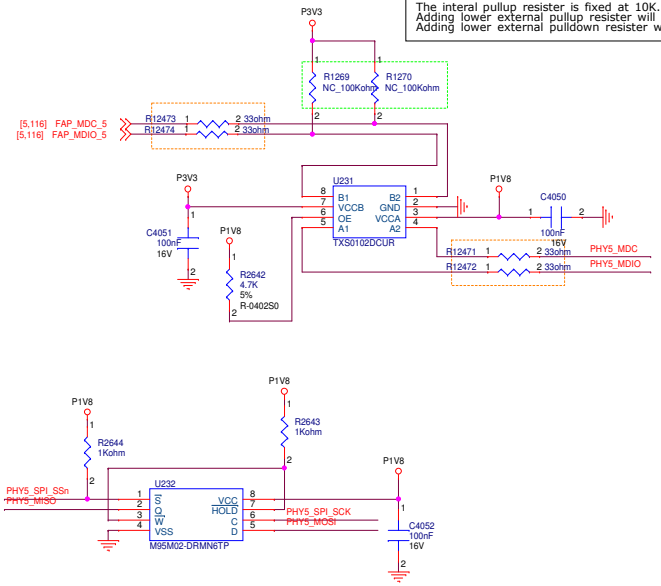
6.3 Recommended Operating Conditions

V_{CC} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

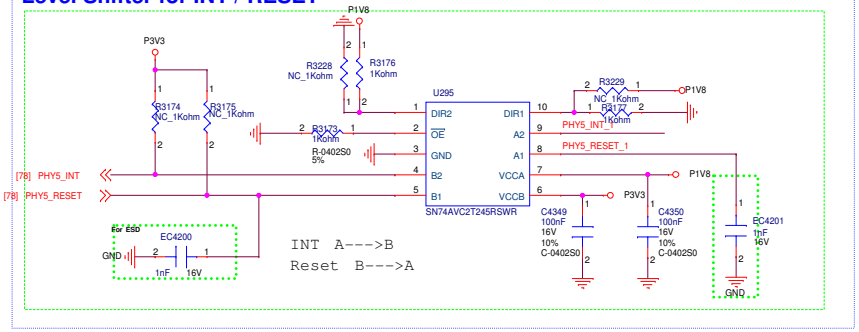
		MIN	MAX	UNIT
V_{CCA}	Supply voltage[1]	1.65	3.6	V
V_{CCB}	Supply voltage	2.3	5.5	V

Note:

The interal pullup resister is fixed at 10K.
Adding lower external pullup resister will effect VOL levels.
Adding lower external pulldown resister will effect VOH levels.



Level Shifter for INT / RESET

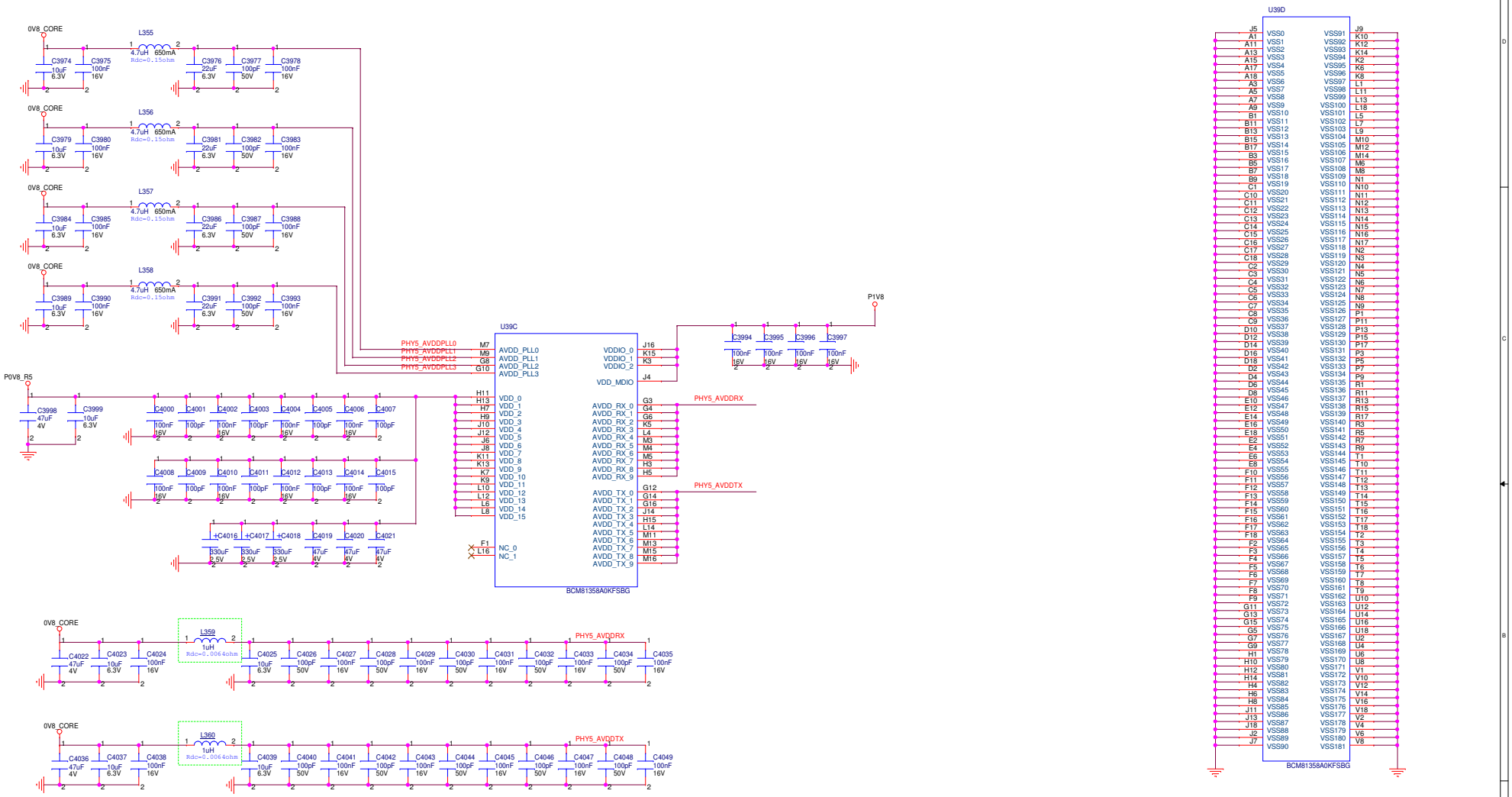


<Core Design>

UfiSpace Co., Ltd.

Title: 118_BCM81358_PHY5_Ac

Document Number:		Sheet	Rev
PCB P/N: T99O114T00		118 of 152	015



<Core Design>

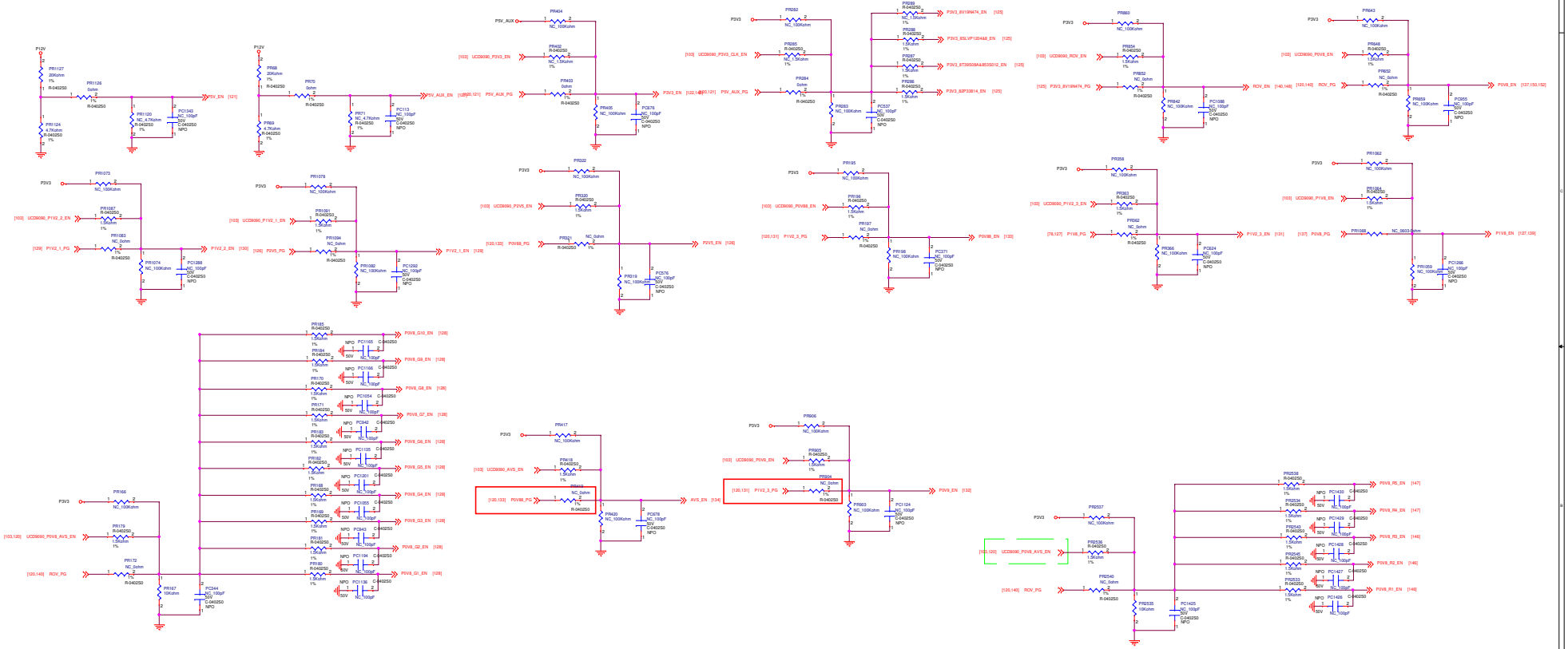
ufiSpace UfiSpace Co., Ltd.

Title

119_BCM81358_PHY5_B

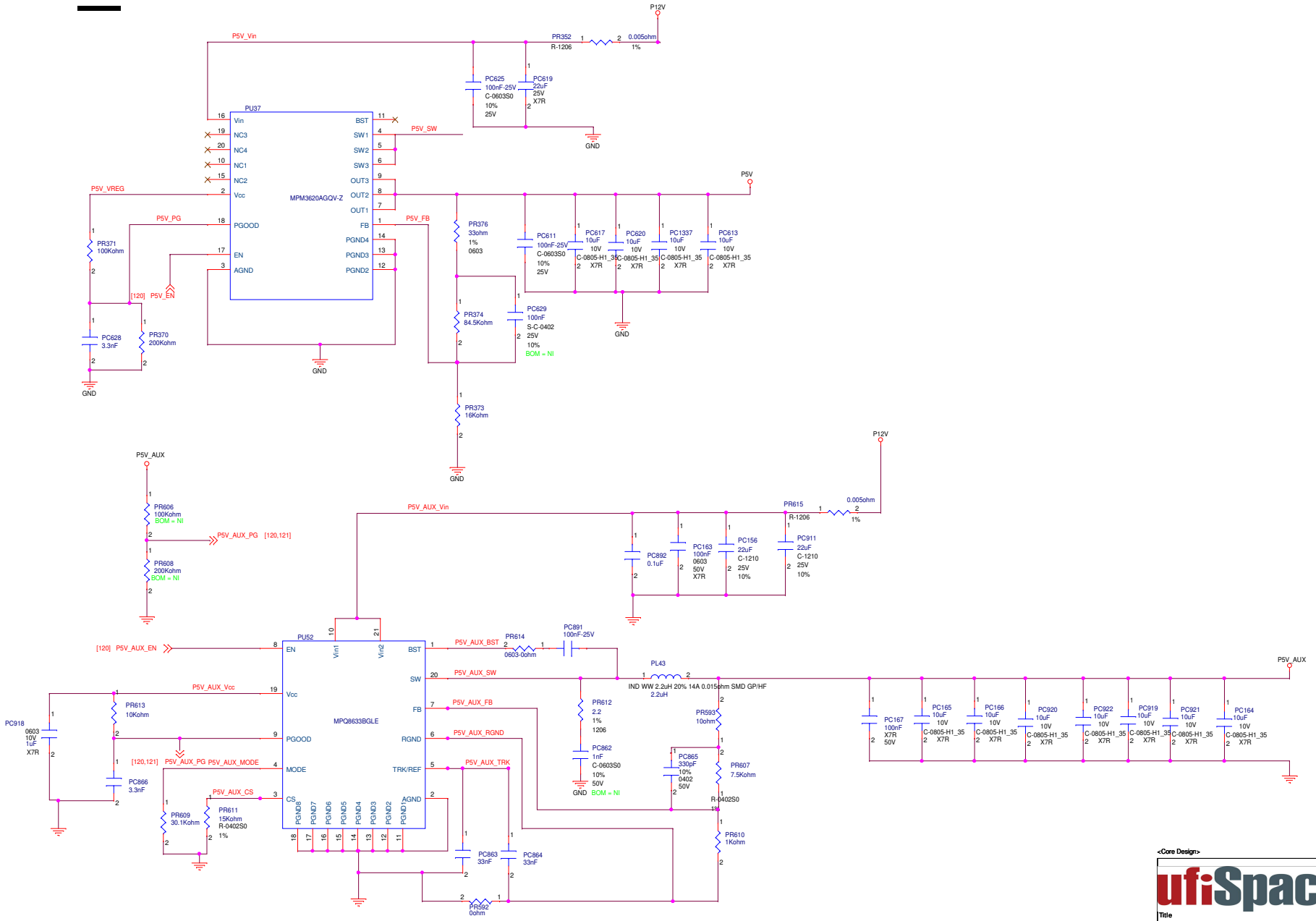
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	119 of 152	015

Power up Sequence



P5V/1A

P5V_AUX/4A



<Core Design>

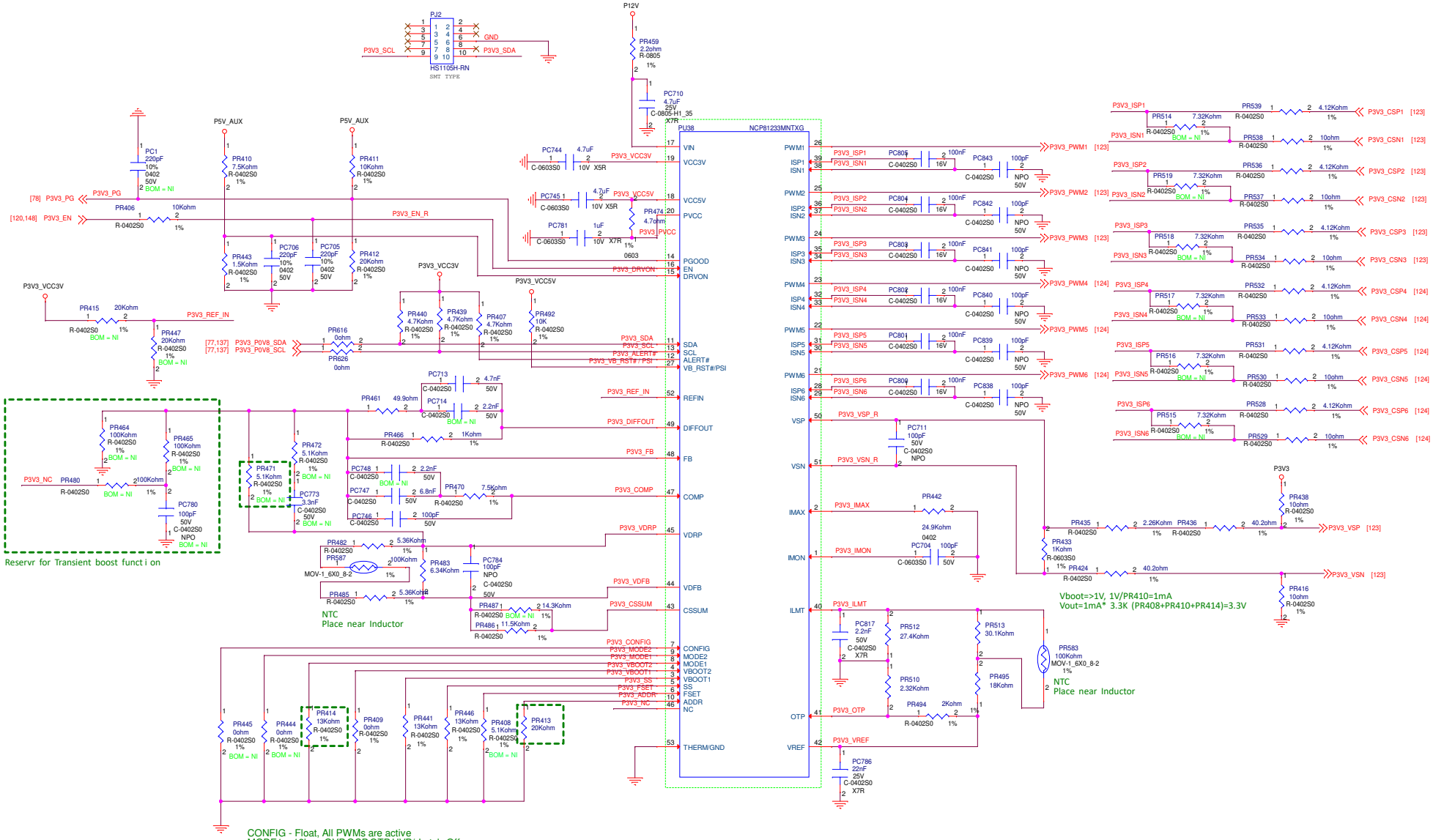
UfiSpace Co., Ltd.

Title

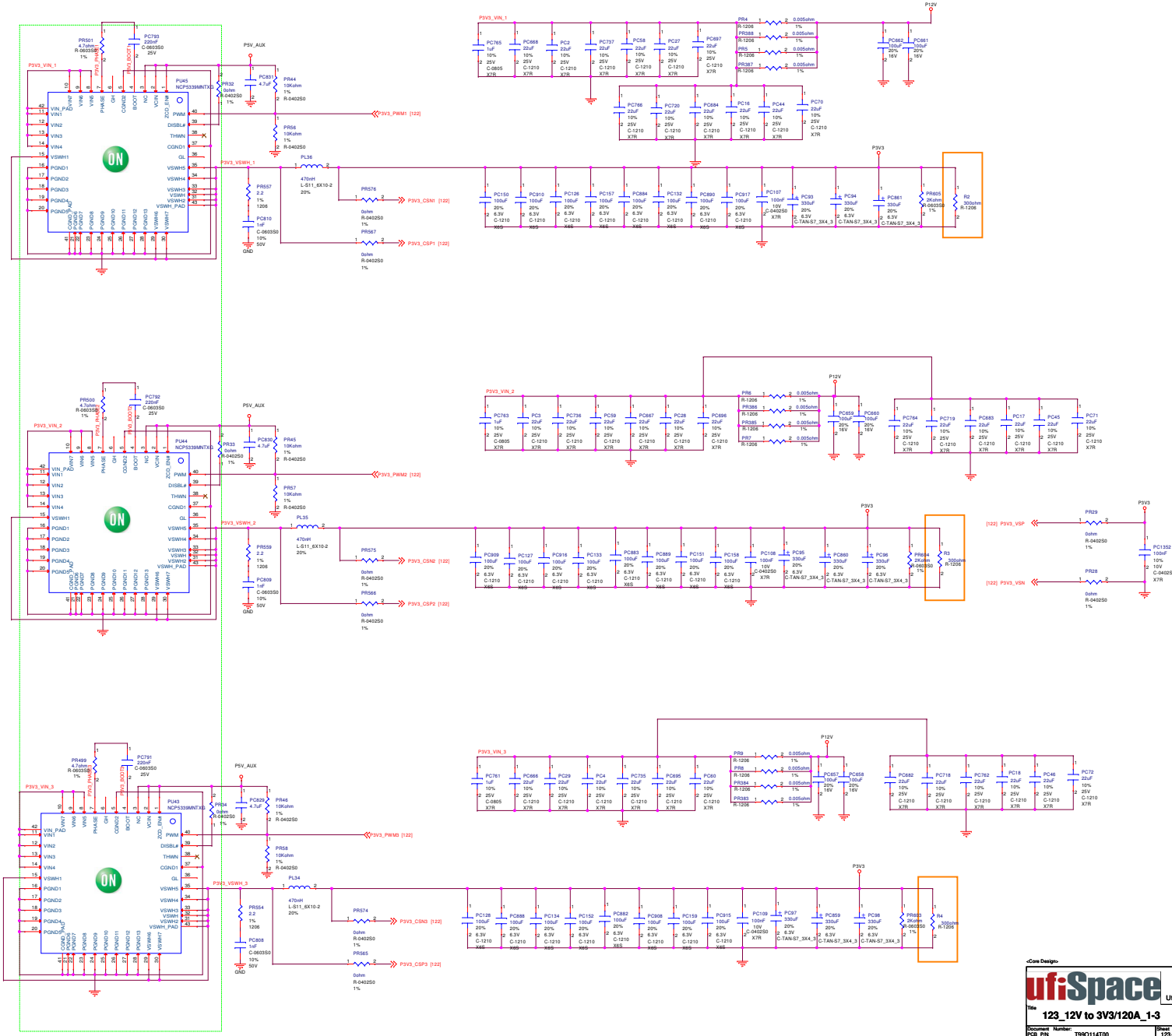
121_12V to 5V

Document Number:		Sheet	Rev
PCB P/N: T99O114T00		121 of 152	015

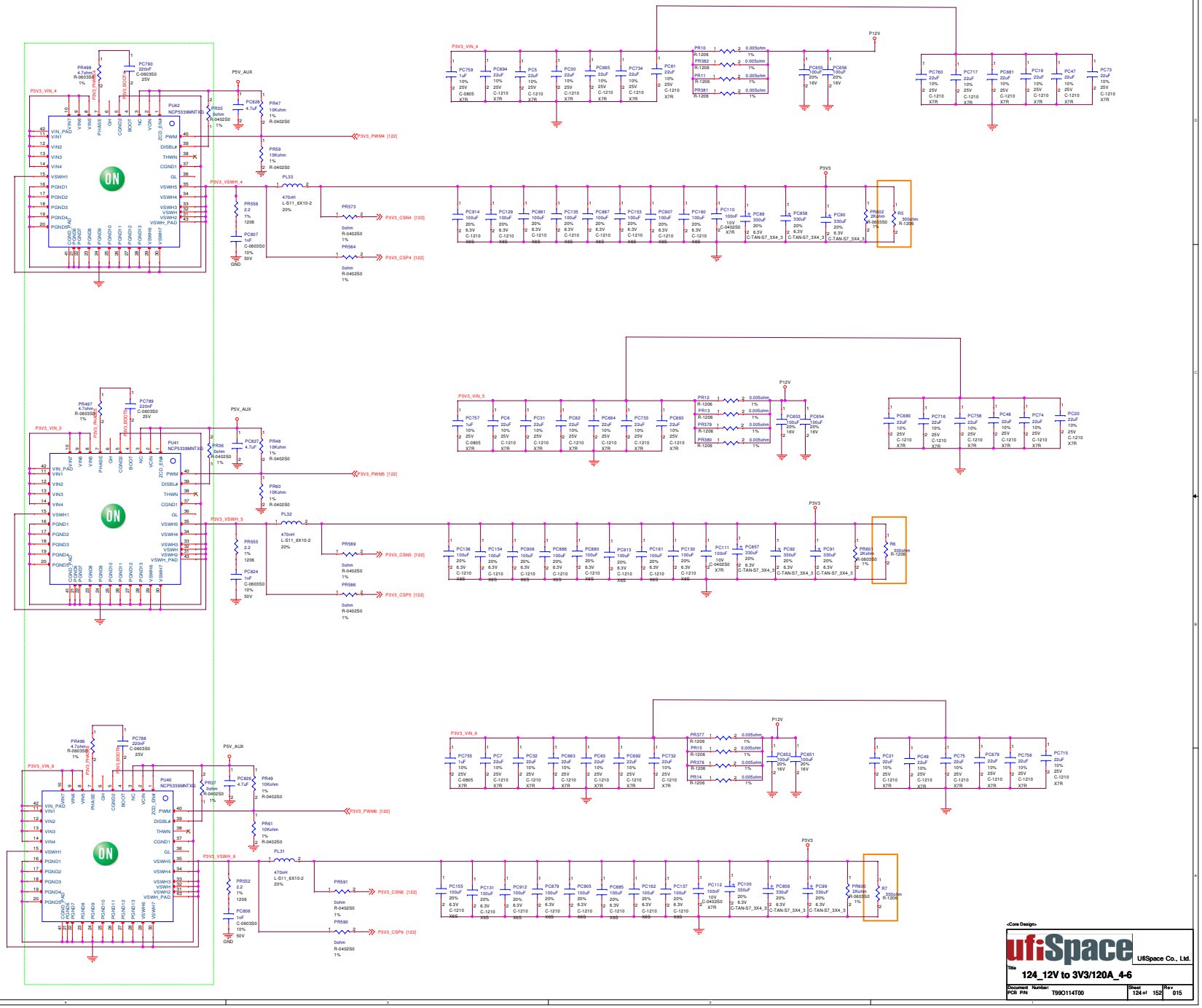
3.3V/120A_controller
Address: 0x76



3.3V/120A_Phase1~3



3.3V/120A_Phase4~6

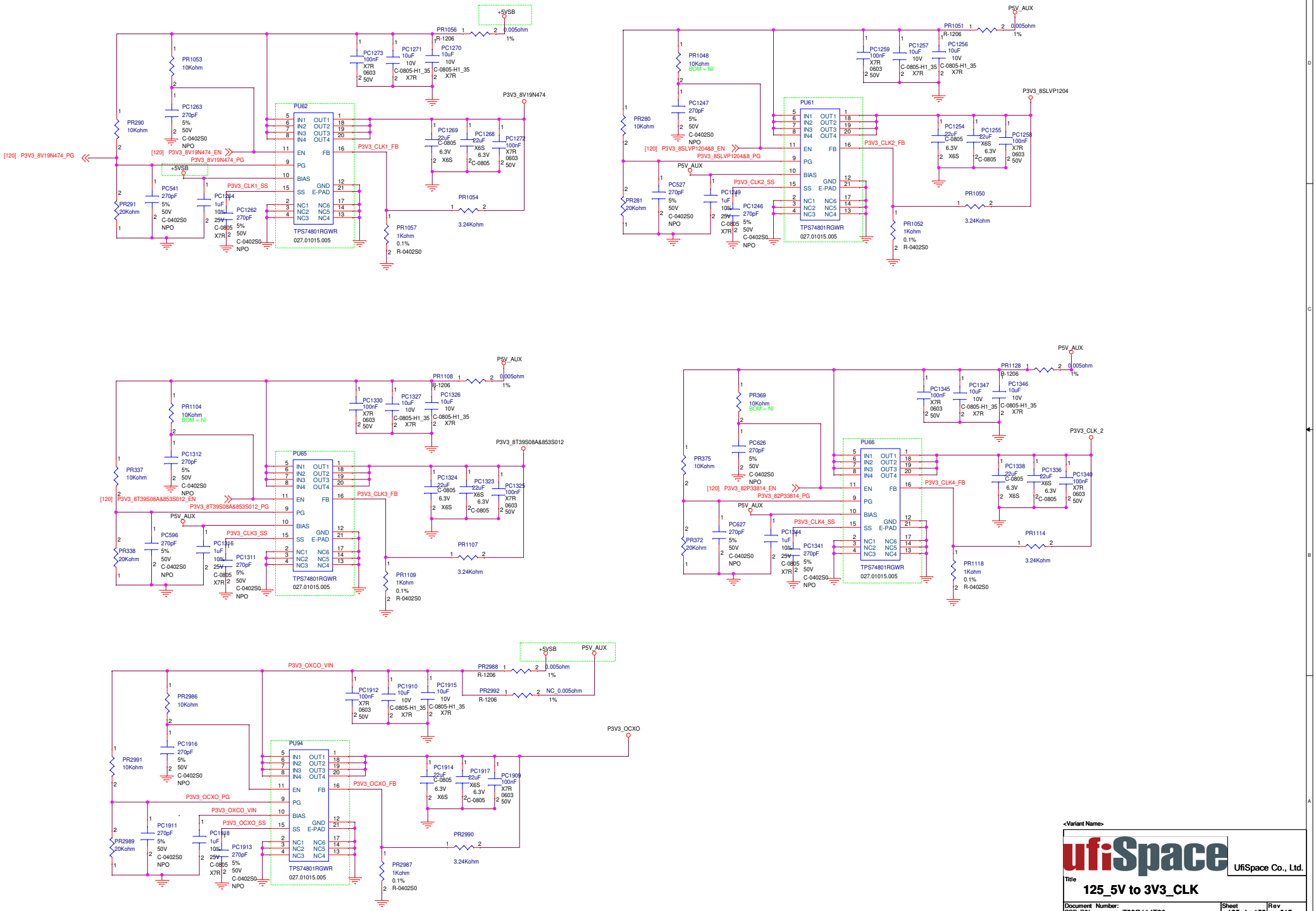


<Core Design>
UfiSpace Co., Ltd.

Title: 124_12V to 3V3/120A_4-6

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	124 of 152	015

P3V3_CLK



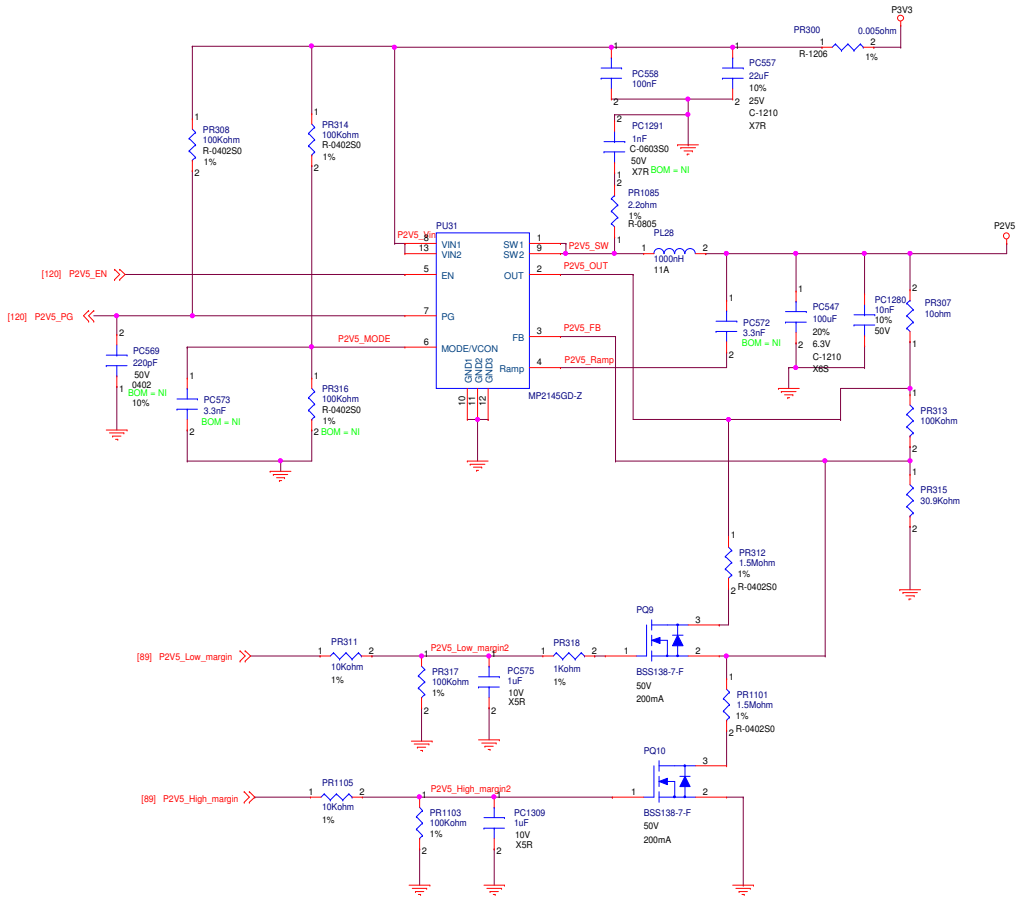
<Variant Name>

UfiSpace Co., Ltd.

Title: 125_5V to 3V3_CLK

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	125 of 152	015

2.5V/1.2A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

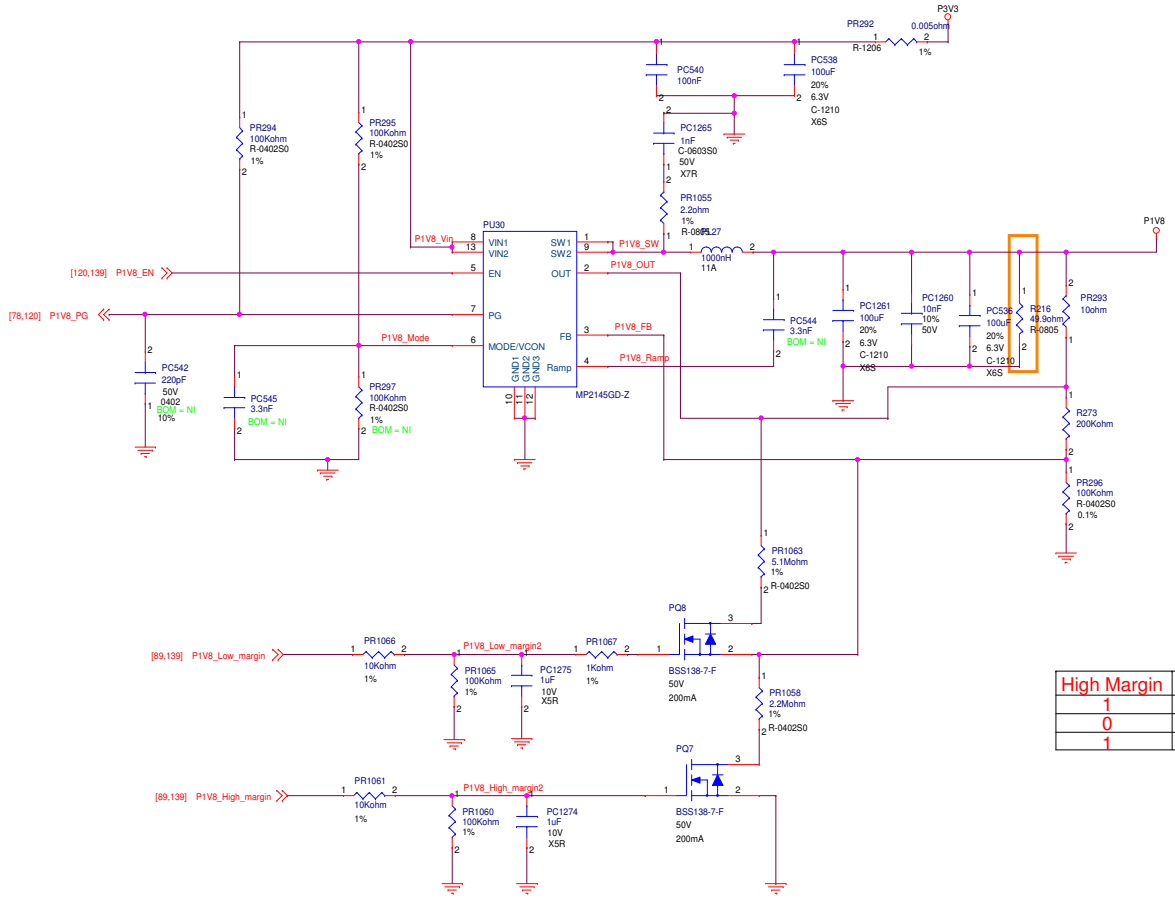
UfiSpace Co., Ltd.

Title

126_3V3 to 2.5V/1.2A

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	126 of 152	015

P1V8_3A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

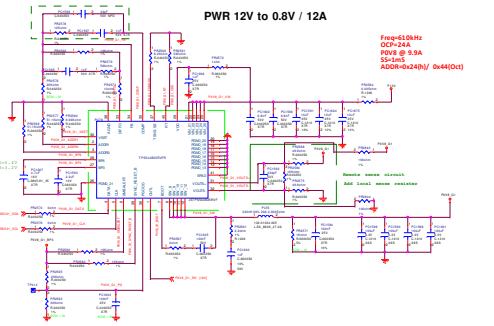
UfiSpace Co., Ltd.

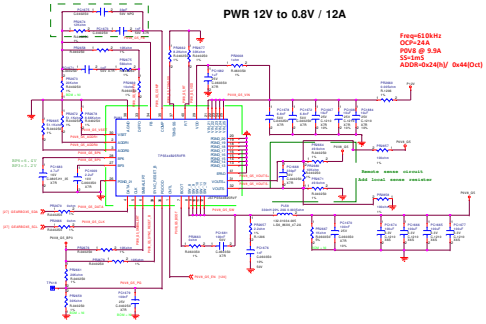
Title

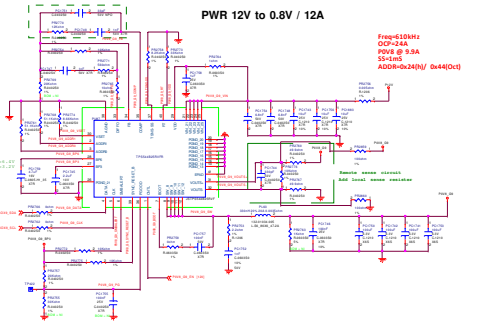
127_3V3 to 1V8/3A

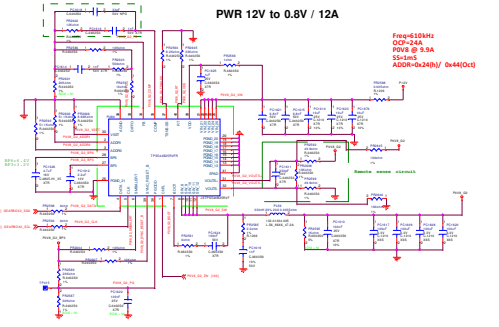
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	127 of 152	015

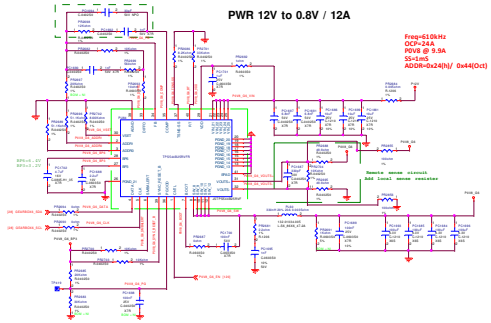
P0V8_Gearbox /12A*10
Peak current:15A*10
Adress:24H

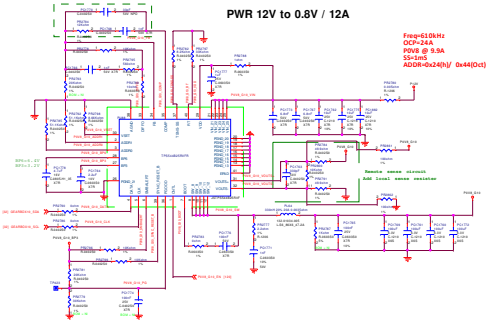


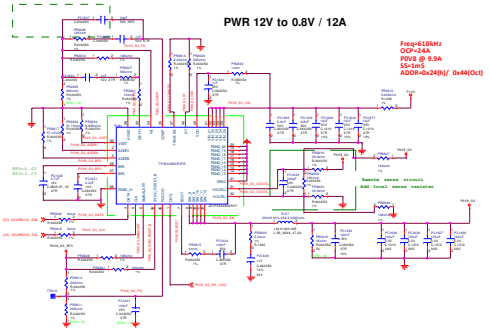


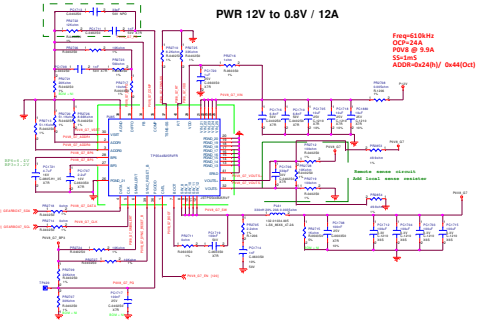


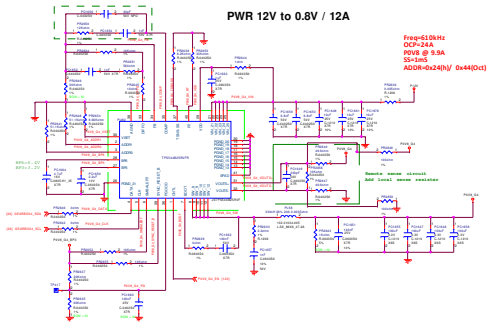


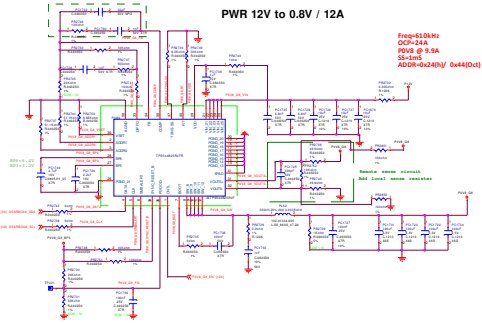






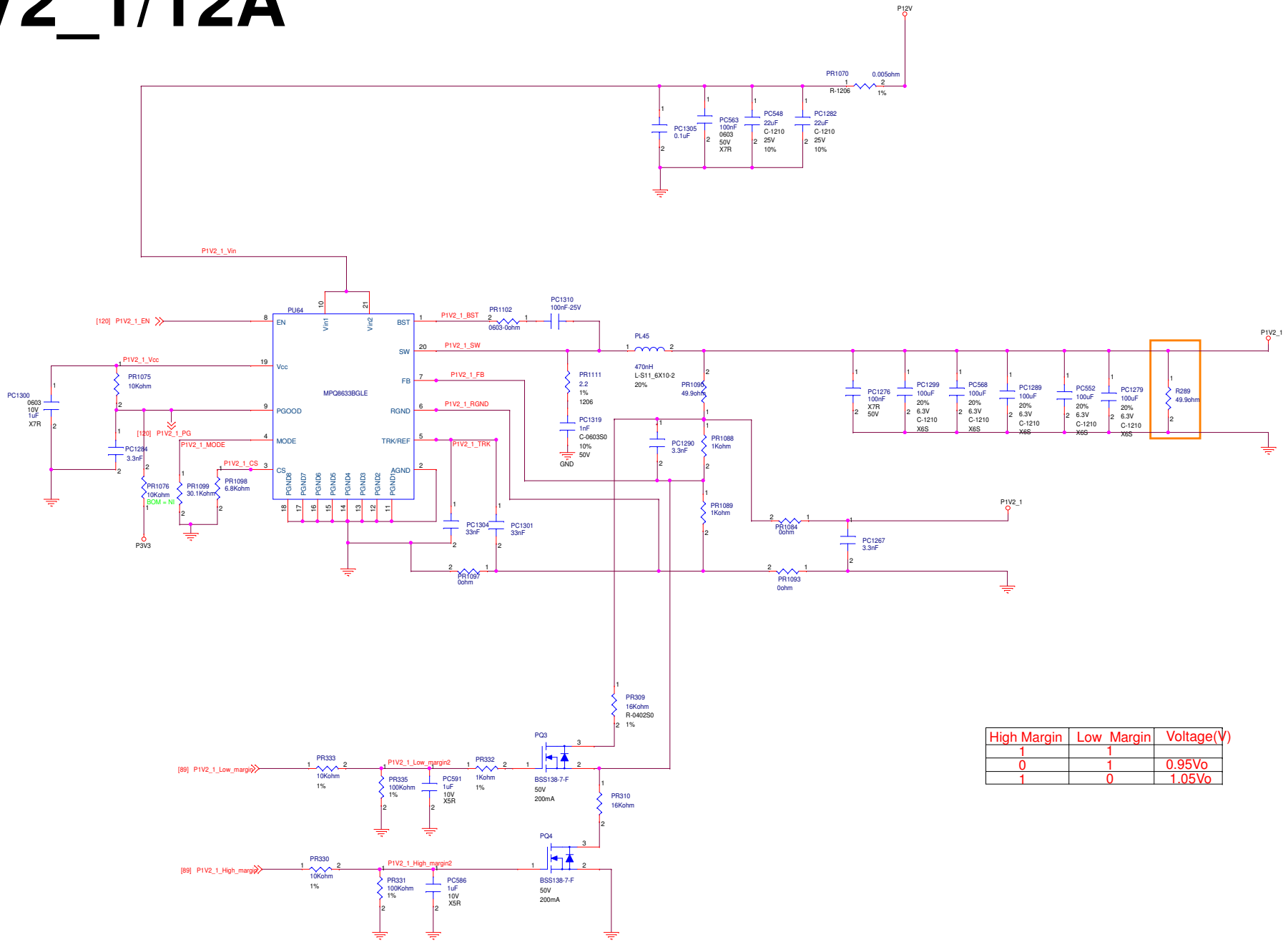






ufiSpace
ufiSpace Co., Ltd
128_12V to AVS_0.8V/110A

P1V2_1/12A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

UfiSpace Co., Ltd.

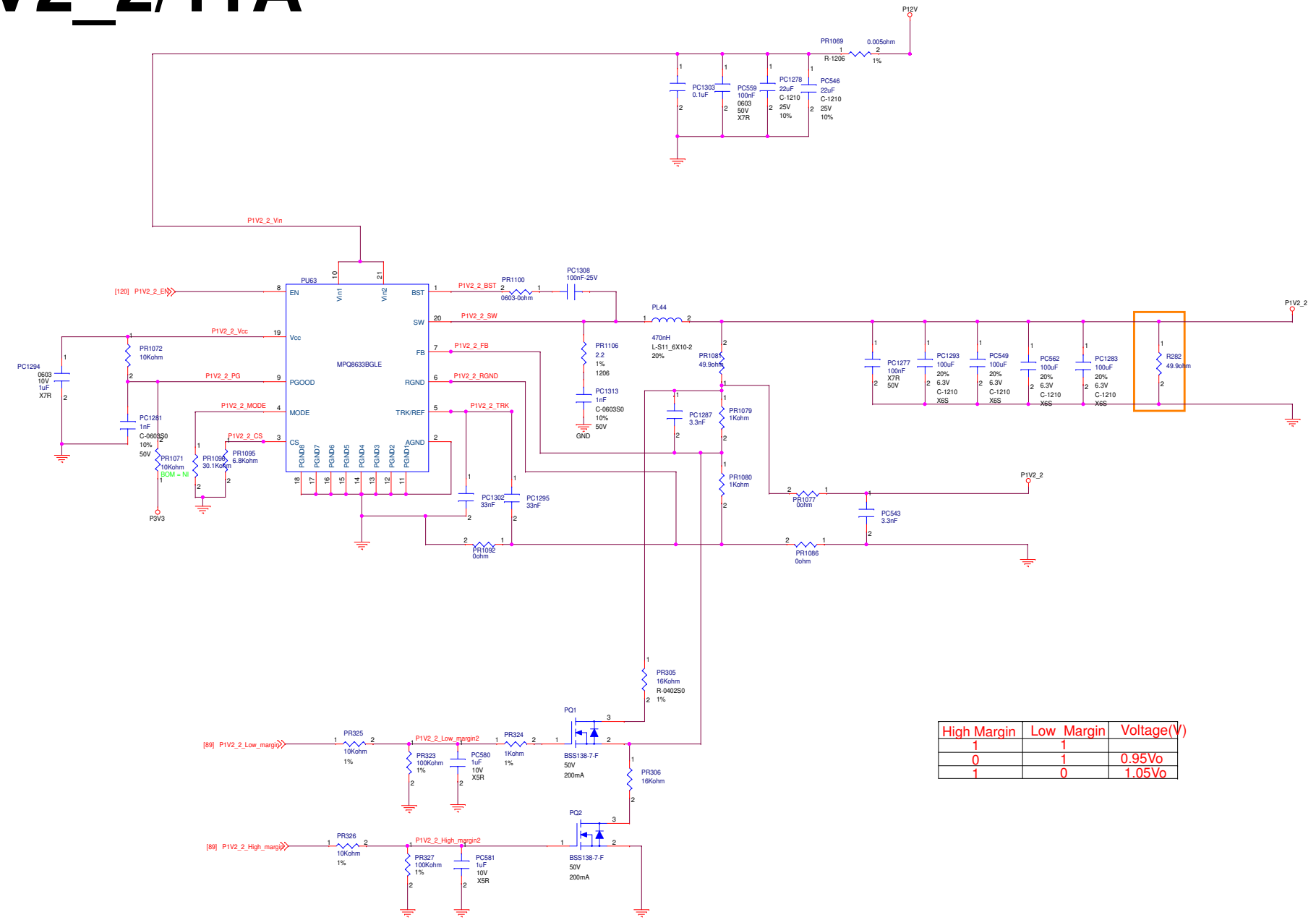
Title: 129_12V to 1V2_1/12A

Document Number: T99O114T00

Sheet 129 of 152

Rev 015

P1V2_2/11A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

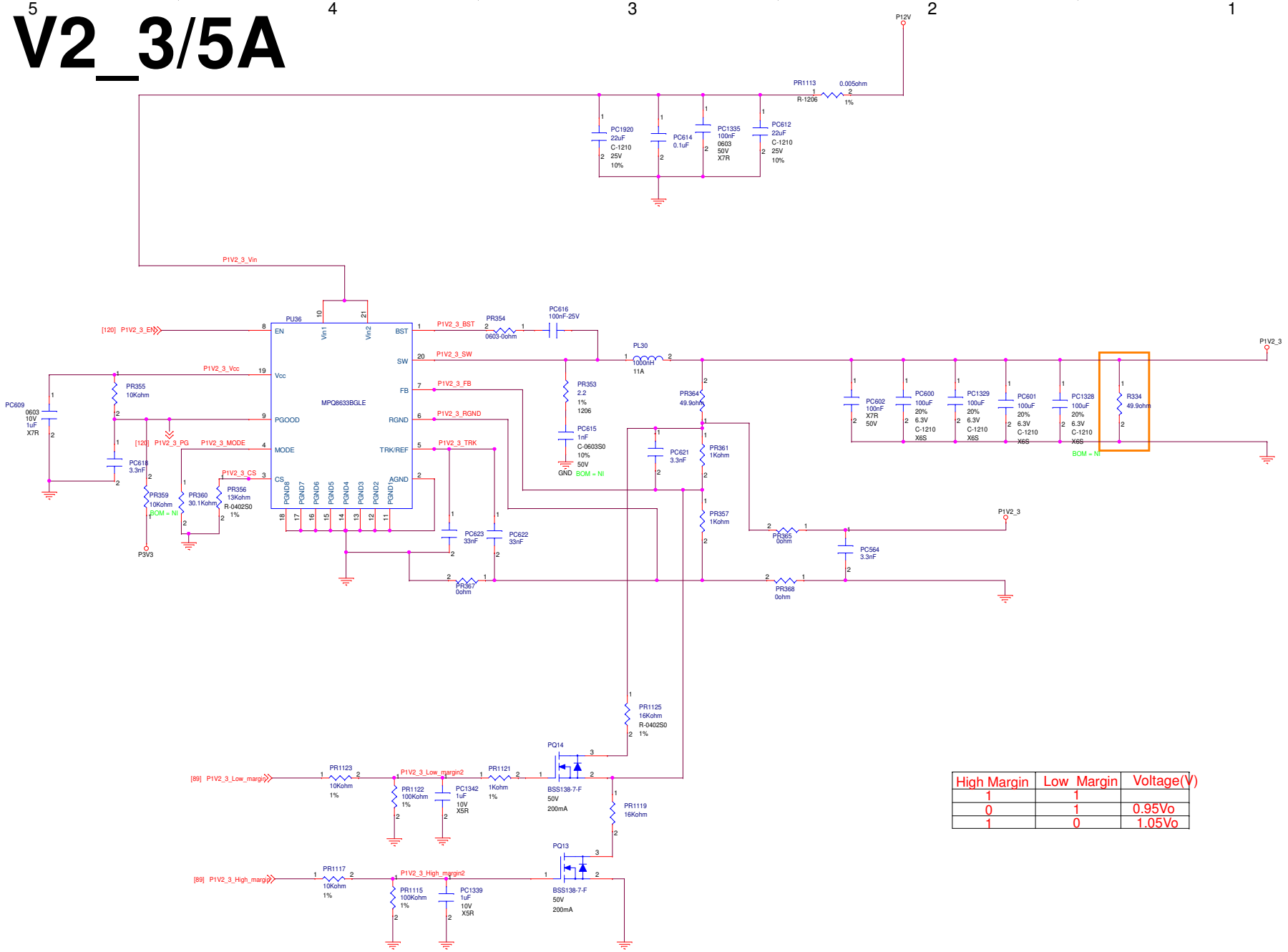
<Core Design>

UfiSpace Co., Ltd.

Title: 130_12V to 1V2_2/11A

Document Number: T99O114T00 | Sheet 130 of 152 | Rev015

P1V2_3/5A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

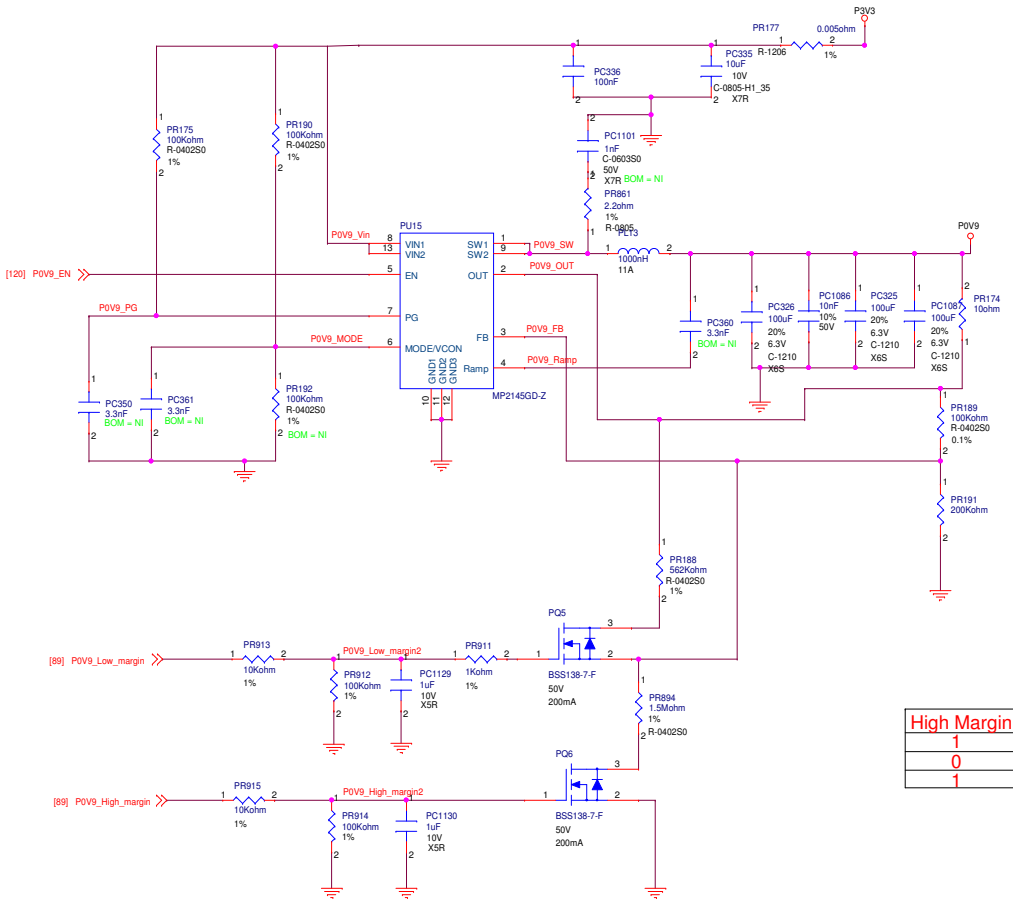
<Core Design>

UfiSpace Co., Ltd.

Title: 131_12V to 1V2_3/5A

Document PCB P/N: T99O114T00 | Sheet 131 of 152 | Rev 015

P0V9_1A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

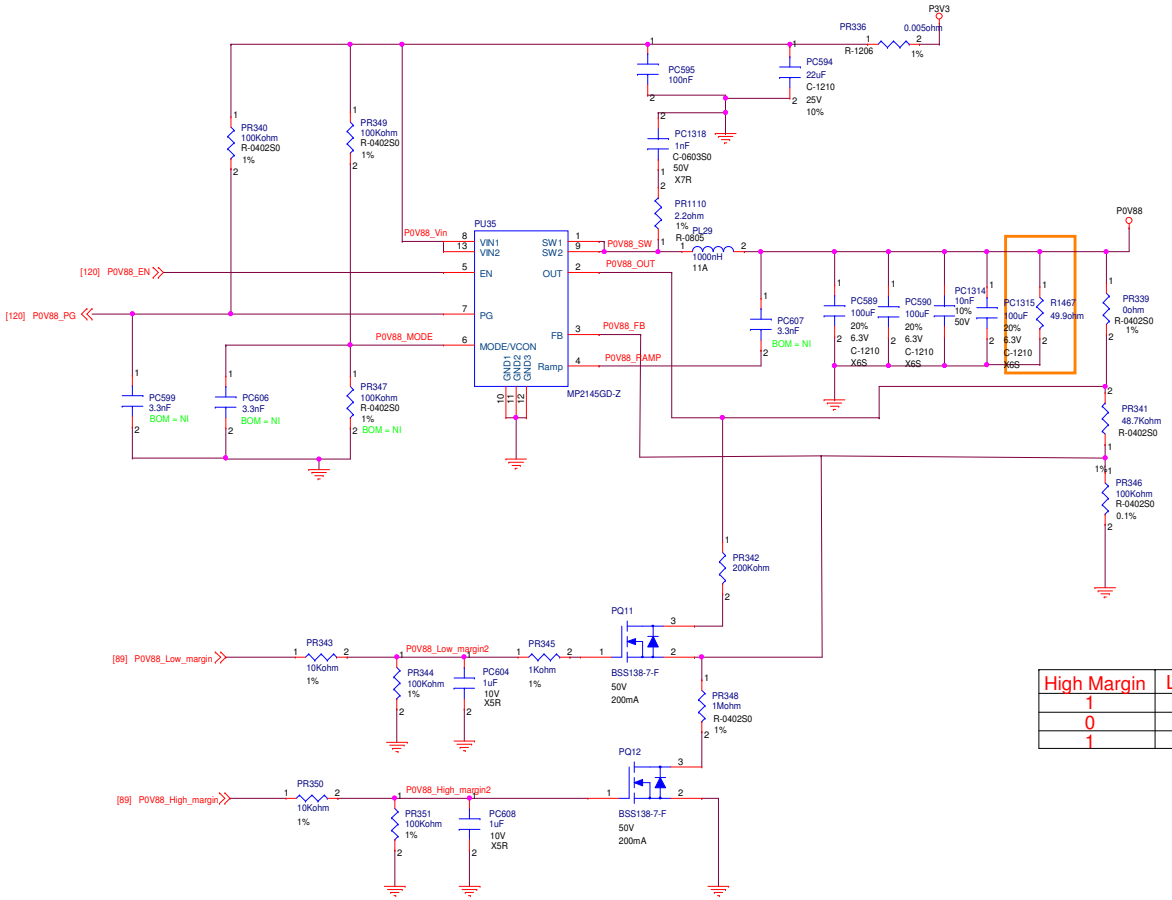
UfiSpace Co., Ltd.

Title

132_3V3 to 0.9V/1A

Document Number: PCB P/N:	Sheet	Rev
T99O114T00	132 of 152	015

P0V88_4A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

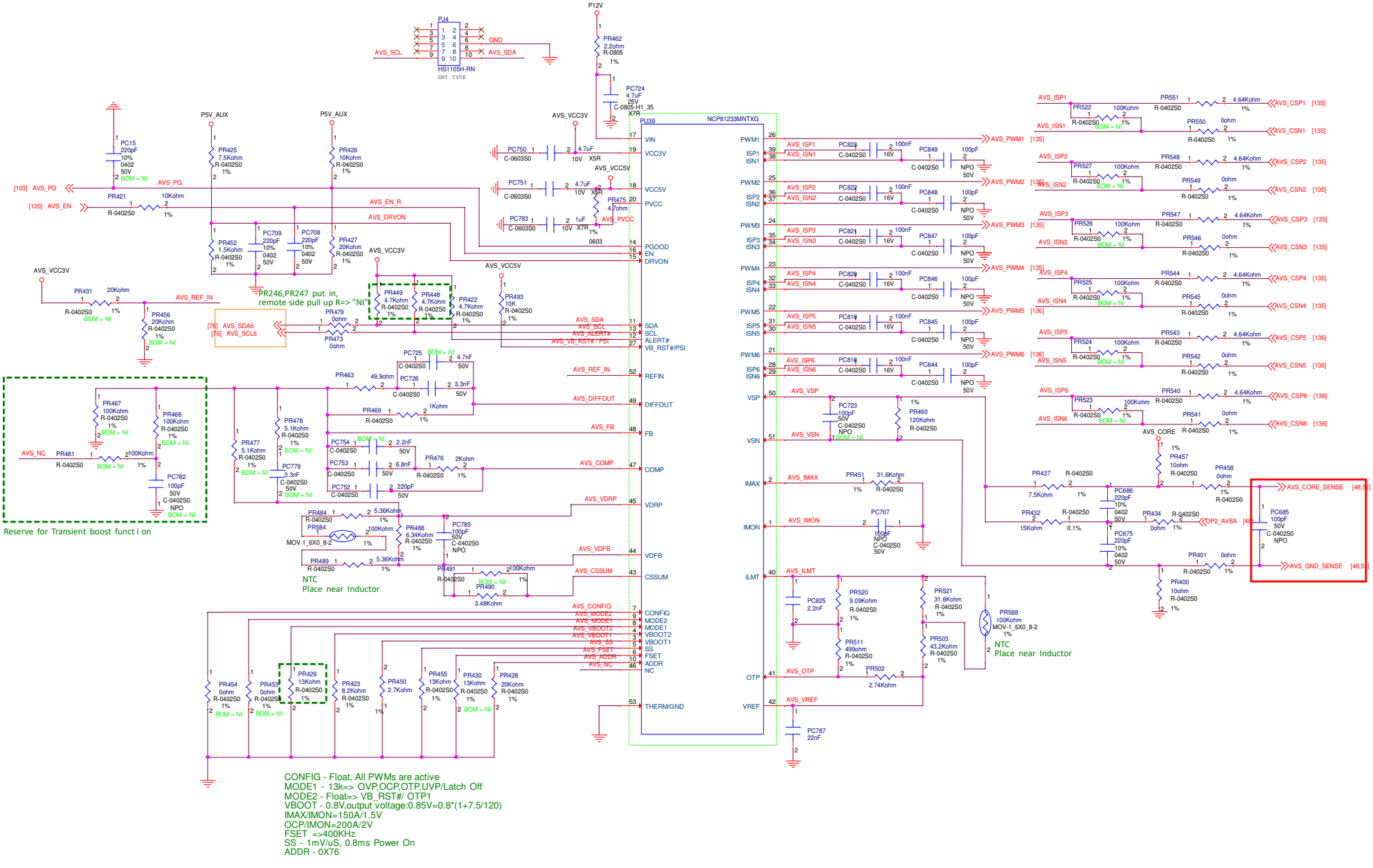
UfiSpace Co., Ltd.

Title

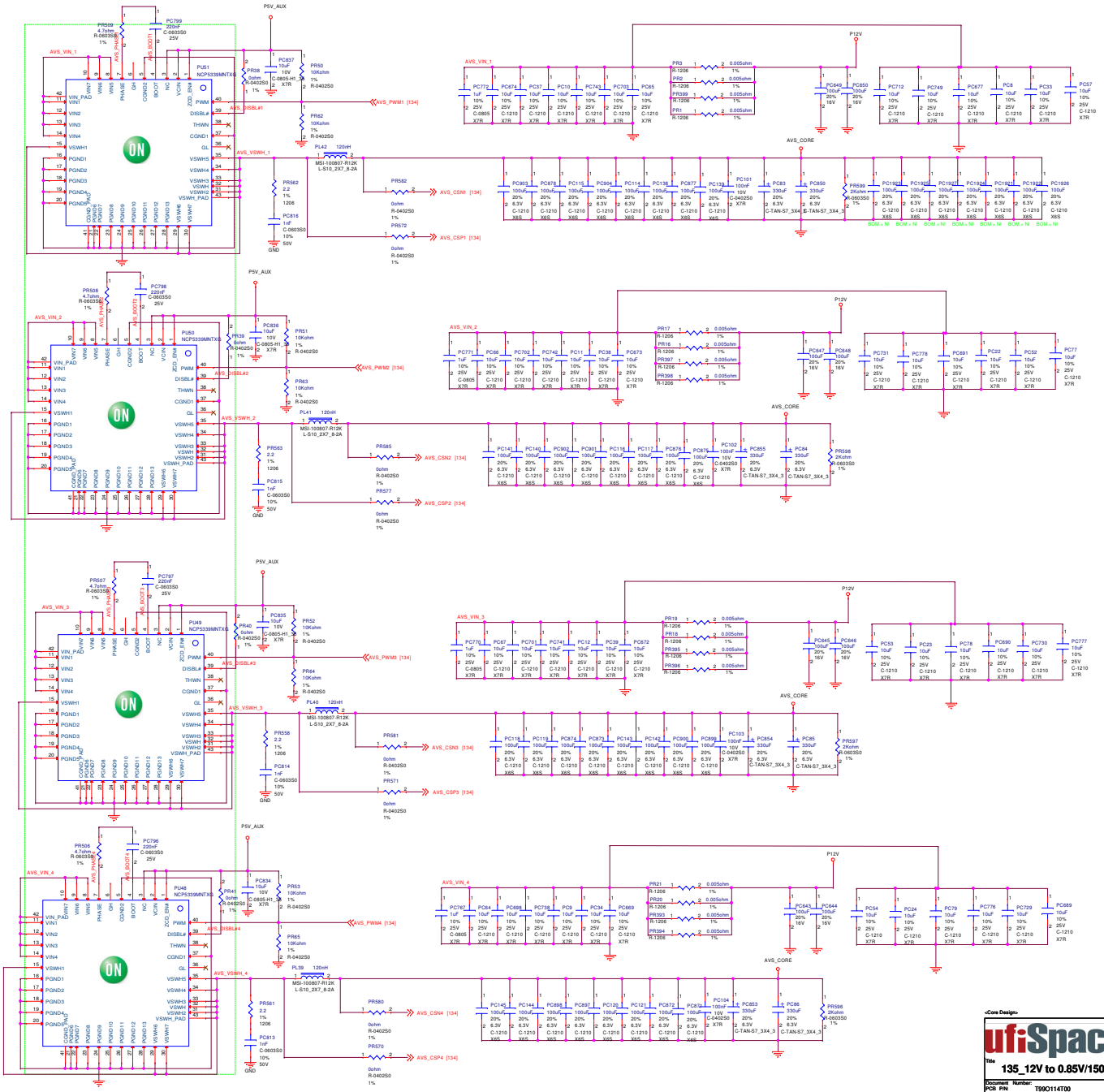
133_3V3 to 0V88/4A

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	133 of 152	015

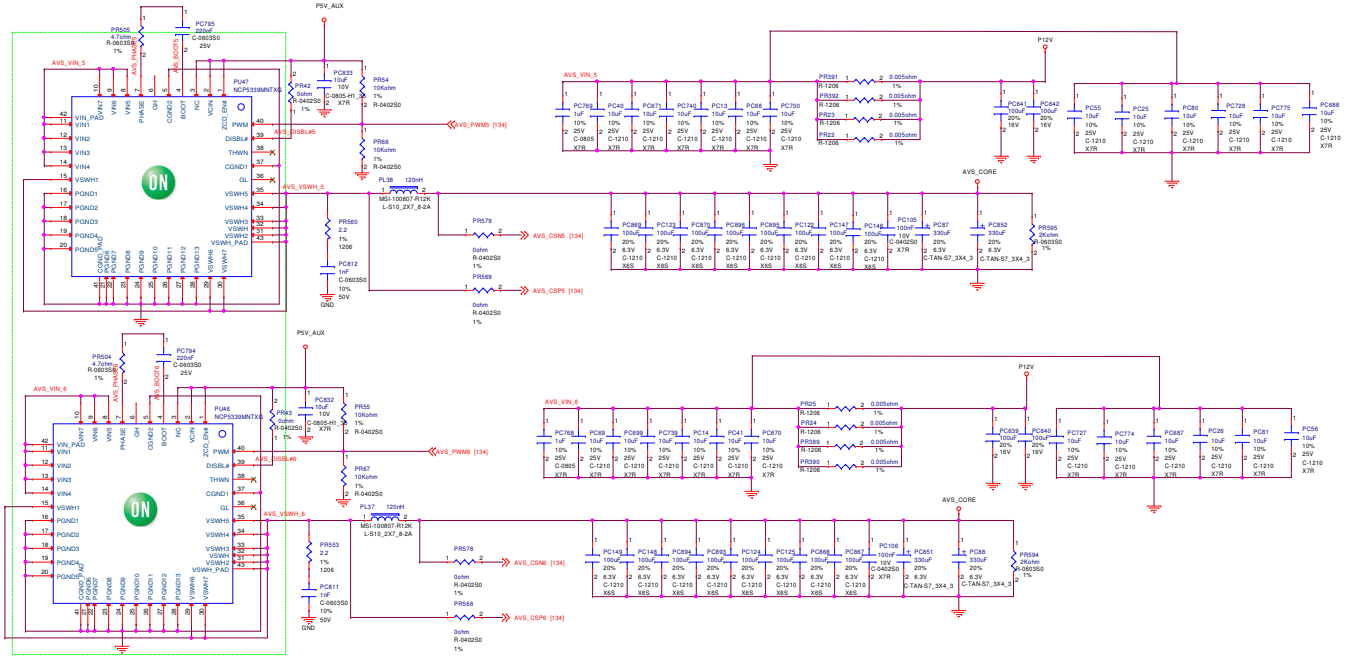
AVS_0.85V /150A_controller
Address: 0X76



AVS_0.85V /150A_Phase 1~4



AVS_0.85V /150A_Phase5~6

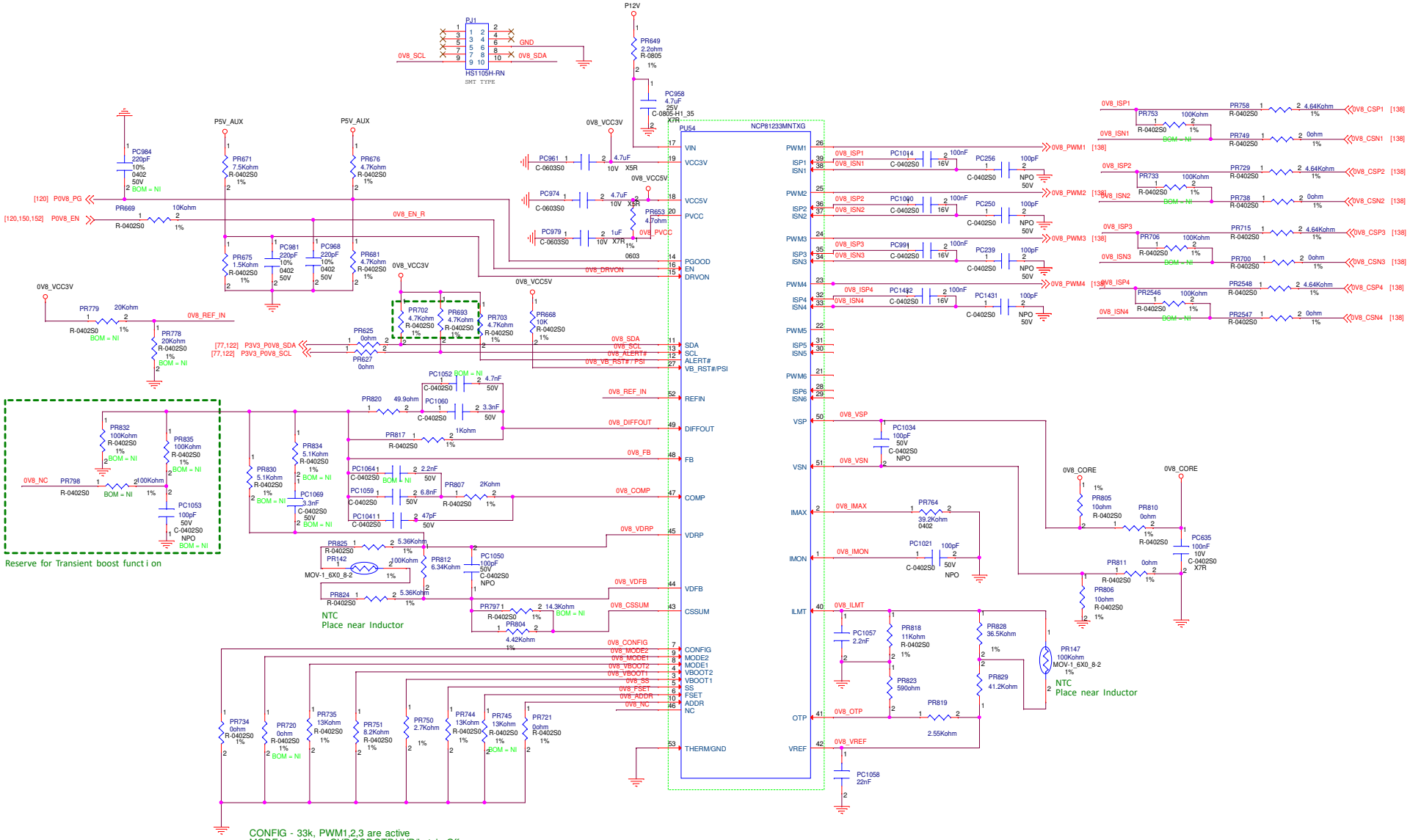


<Core Design>
UfiSpace Co., Ltd.

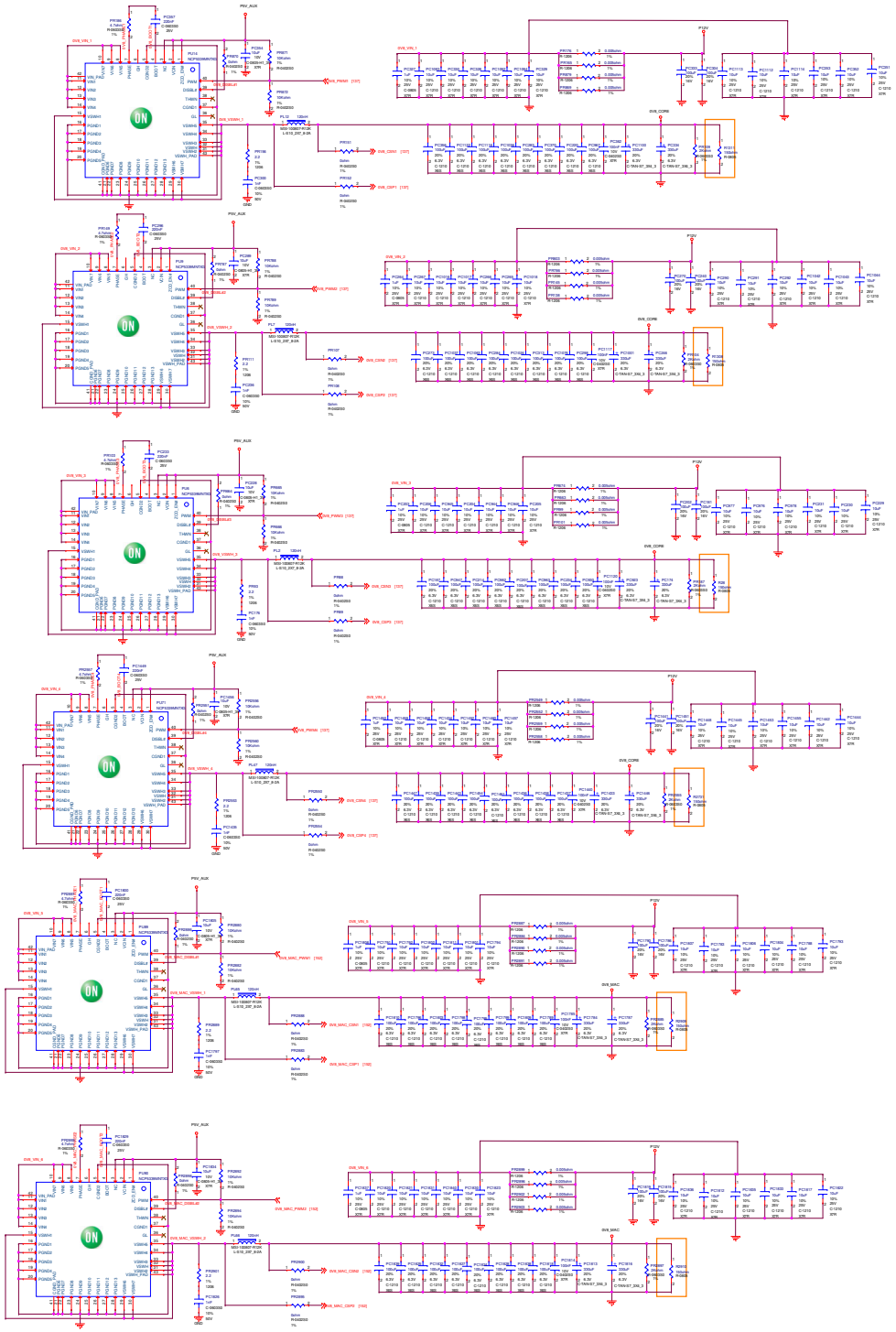
Title: 136_12V to 0.85V/150A_5-6

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	136 of 152	015

0.80V /97A_controller
Address:0x75

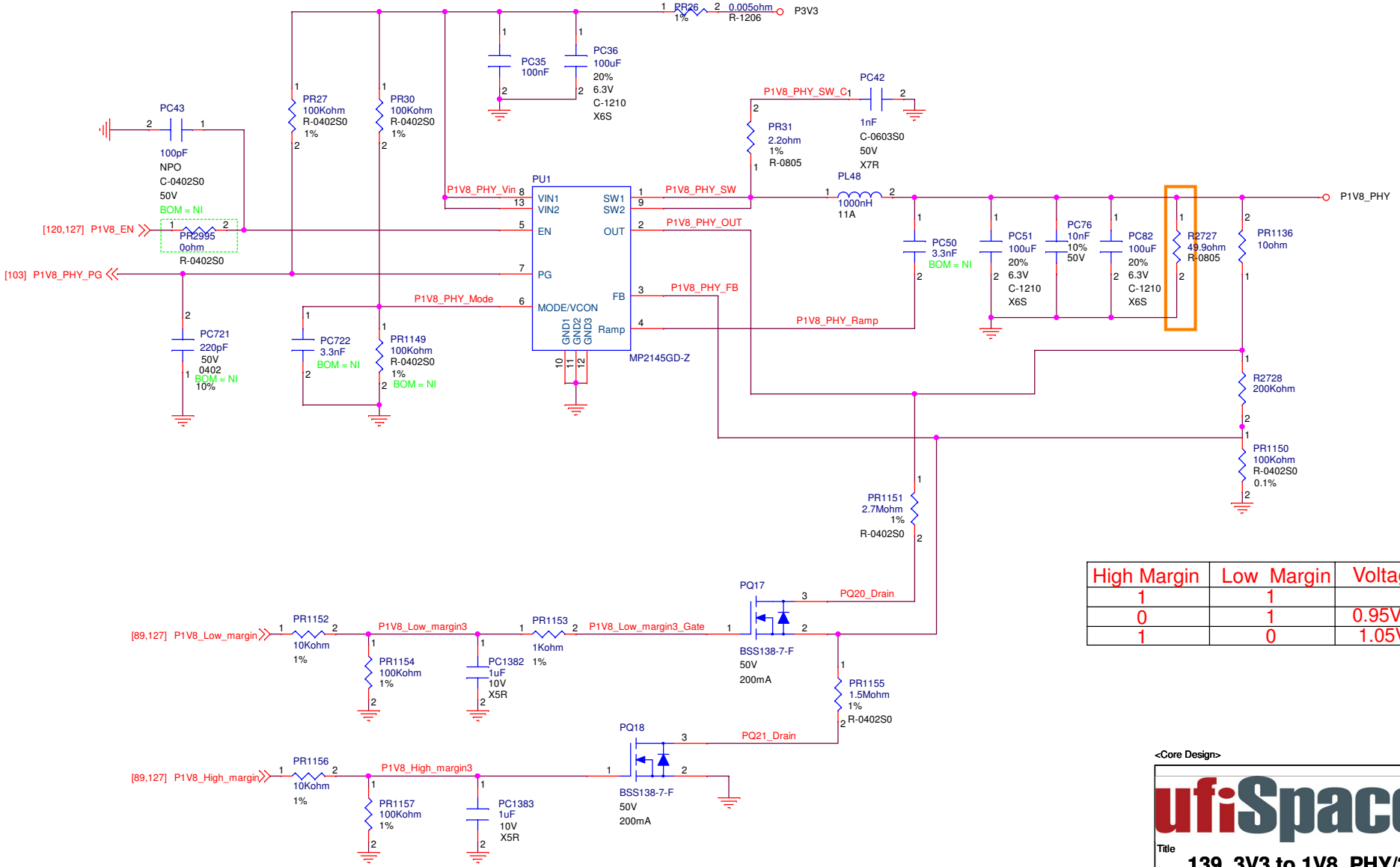


0.80V /127A_Phase1~4



Core Design	ufiSpace UfiSpace Co., Ltd.
Title	138_12V to 0V8/97A_1-4
Drawing No.	T58CH147(0)
Version	138-47
Date	2021/01/15
Sheet	015

P1V8_PHY_0.5A



High Margin	Low_Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

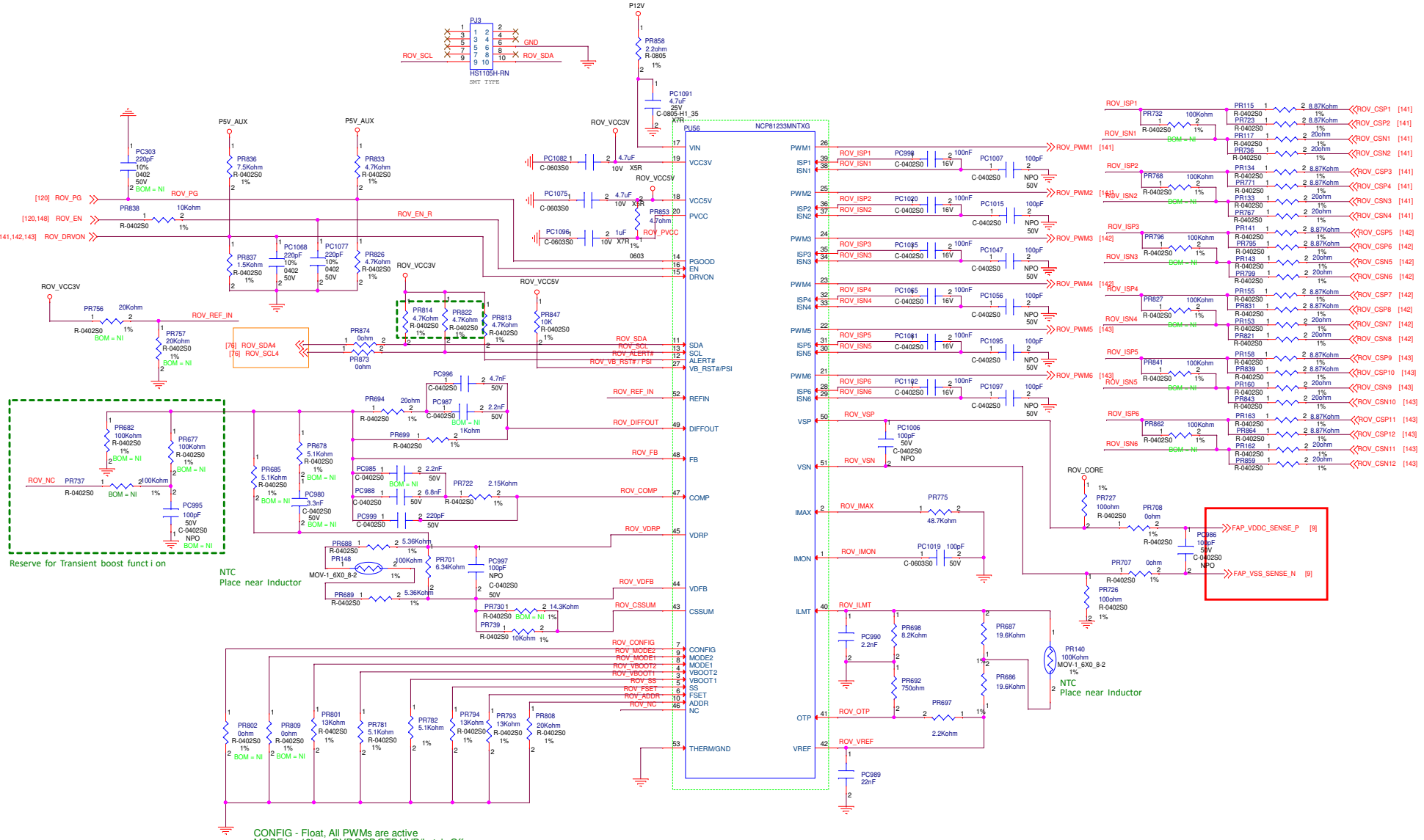
UfiSpace Co., Ltd.

Title

139_3V3 to 1V8_PHY/3A

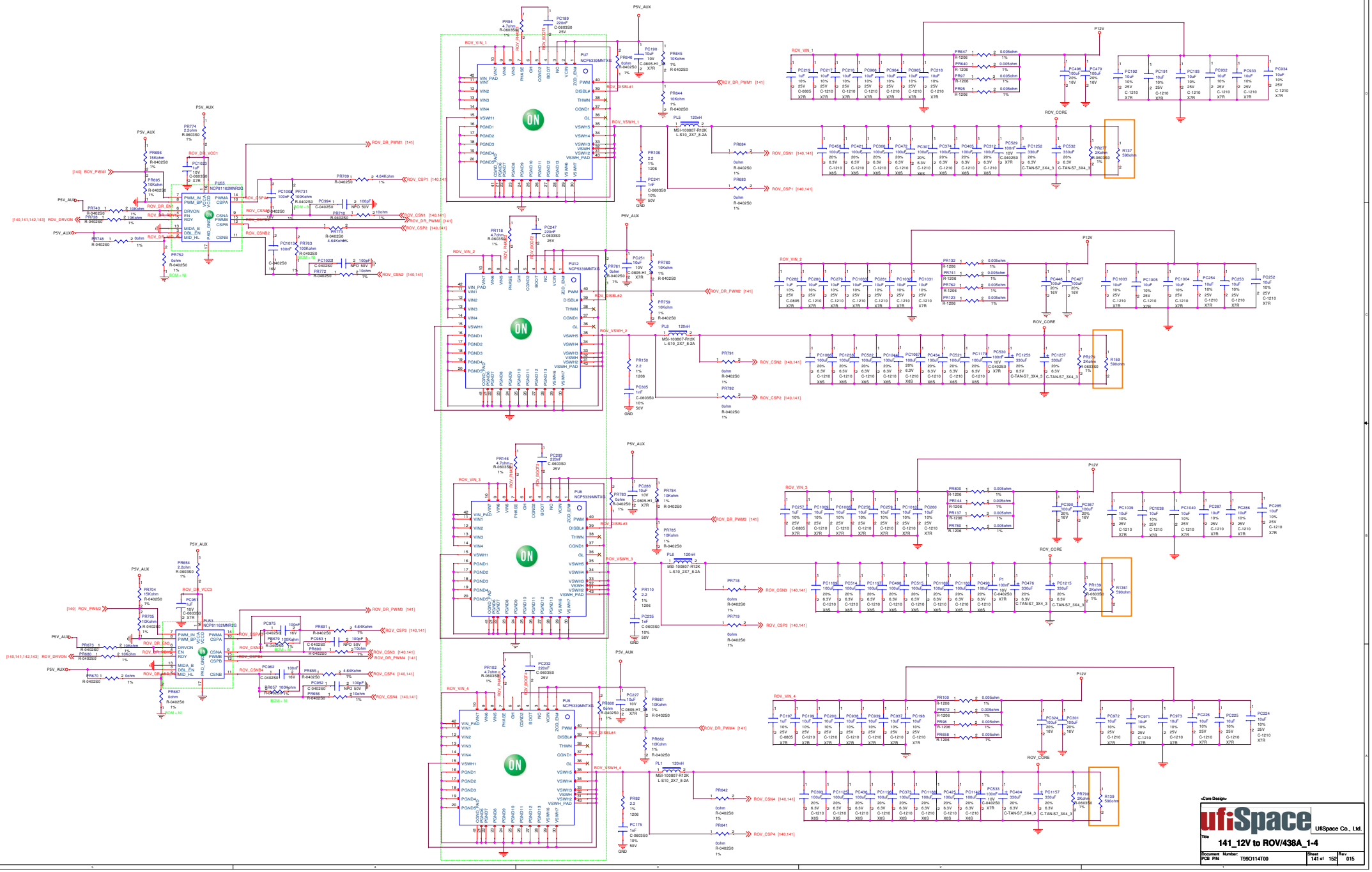
Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	139 of 152	015

0.80V_ROV /438A_Controller
Address:0x76

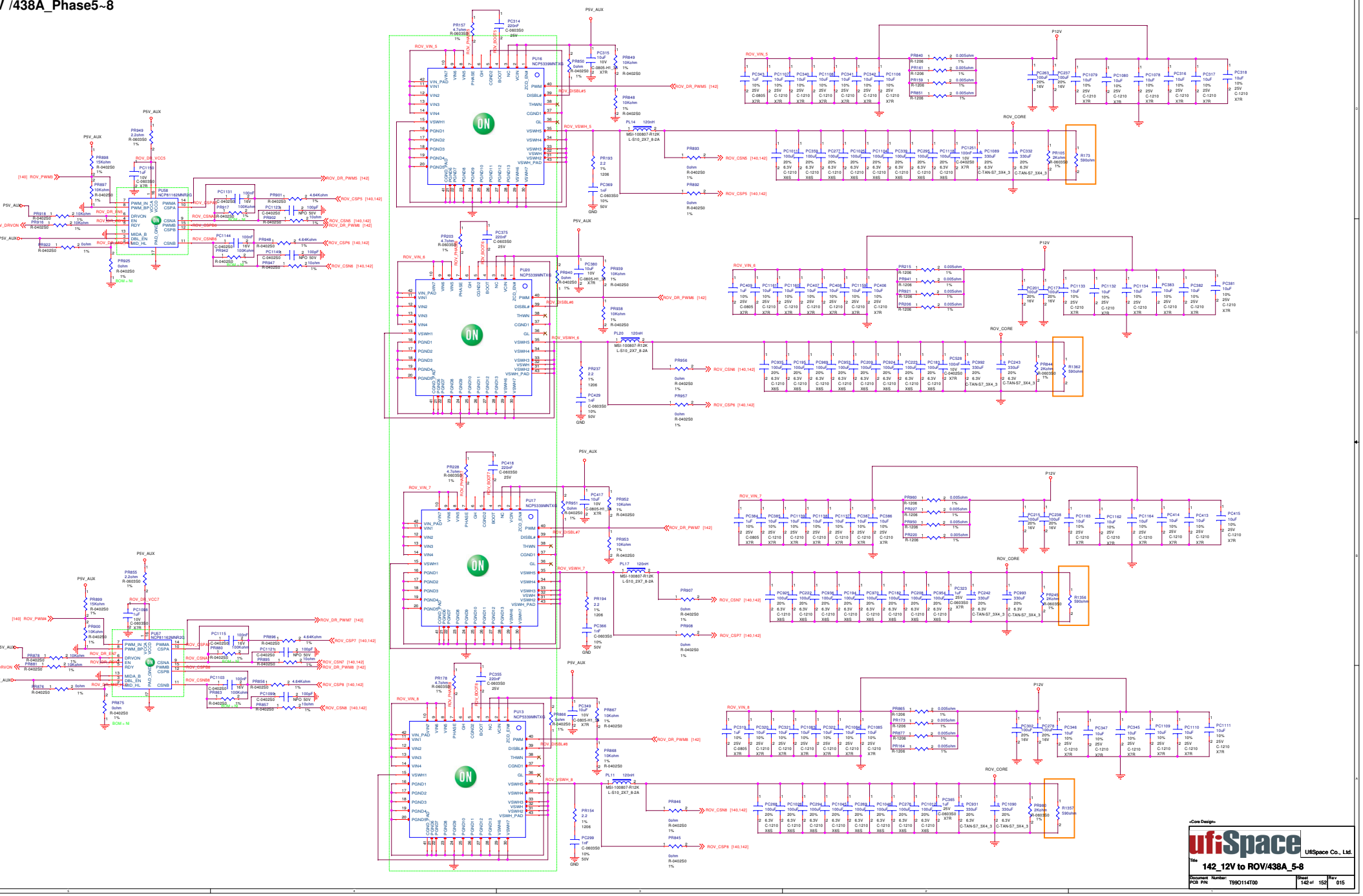


CONFIG - Float, All PWMs are active
MODE1 - 13k=> OVP,OCP,OTP,UVP/Latch Off
MODE2 - Float=> VB_RST#/ OTP1
VBOOT - 0.80V
IMAX/IMON=437A/1.52V
OCP/IMON=574A/2V
FSET - 800KHz / 2=>400KHz
SS - 1mV/uS, 0.8ms Power On
ADDR - 0x76

0.80V_ROV /438A_Phase1~4



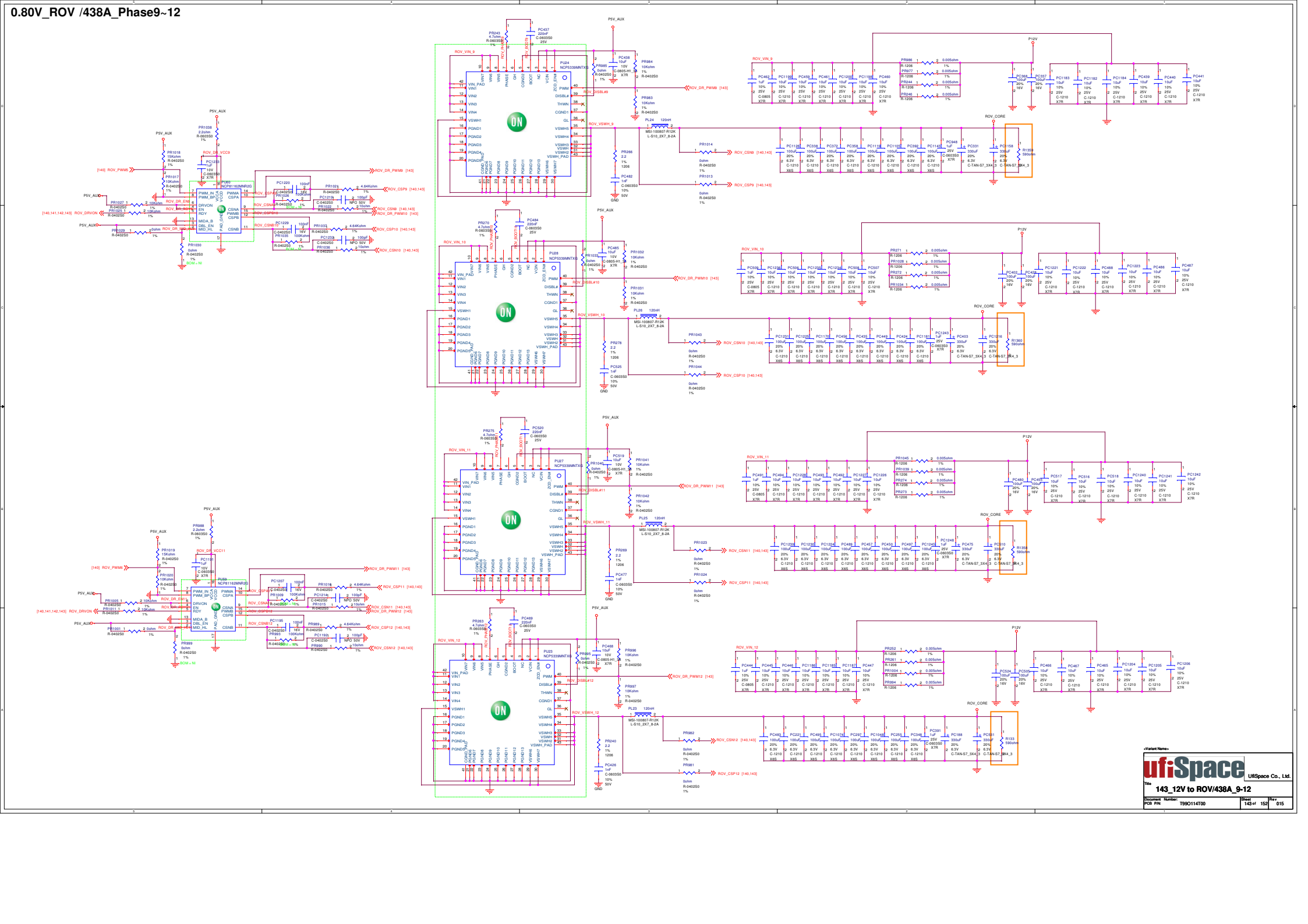
0.80V_ROV /438A_Phase5~8



<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title	142_12V to ROV/438A_5-8		
Document Number: PCB P/N:	T99O114T00	Sheet 142 of 152	Rev 015

0.80V_ROV /438A_Phase9~12



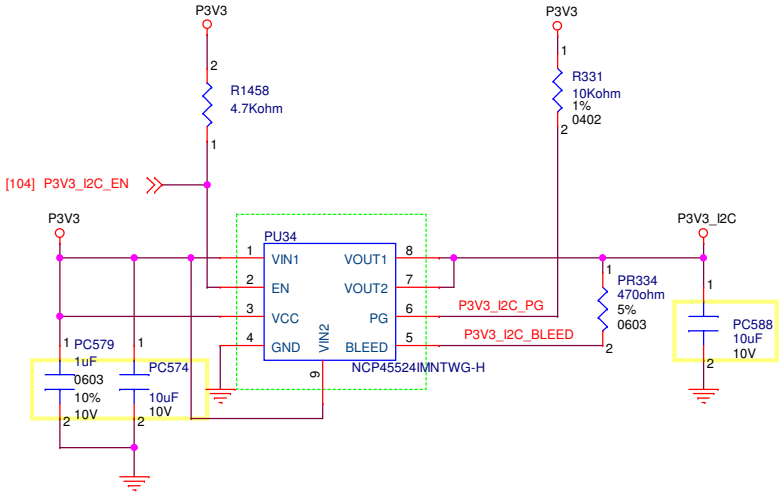
<Variant Name>

ufiSpace

UfiSpace Co., Ltd.

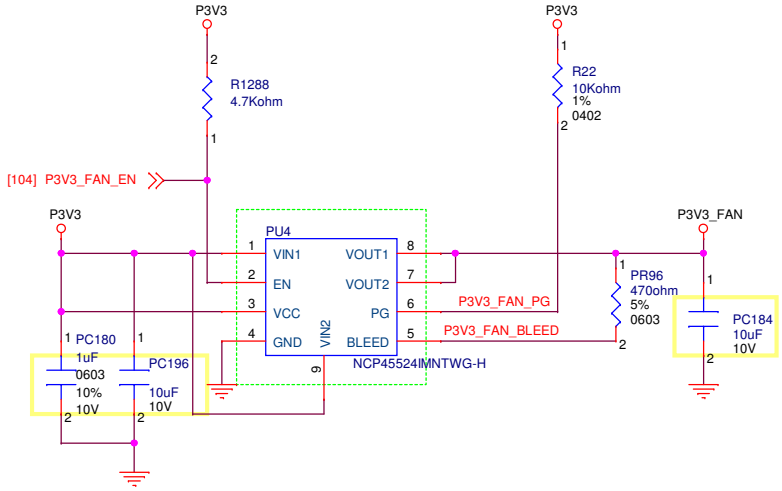
Title: 143_12V to ROV/438A_9-12

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	143 of 152	015



P3V3_I2C_1.6A
Max = 6A

CAD NOTE:
Add divider circuit can make Enable pin not floating,
and to avoid turn on /turn off error action.



P3V3_FAN_0.6A
Max = 6A

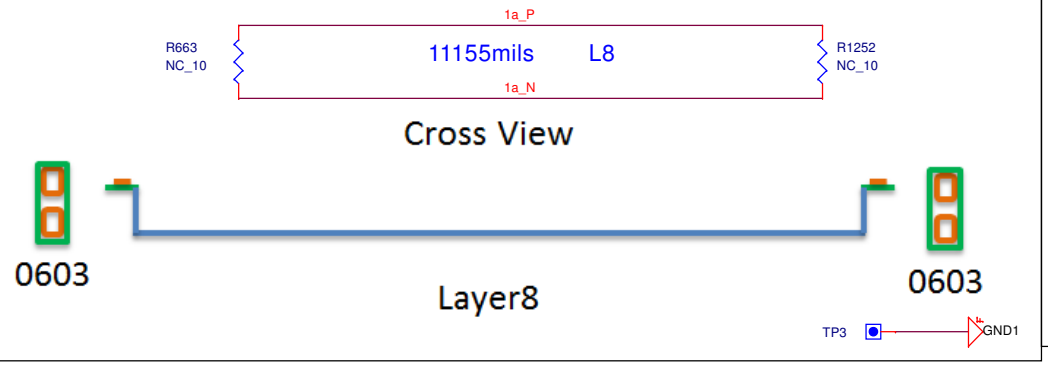
<Core Design>

UfiSpace Co., Ltd.

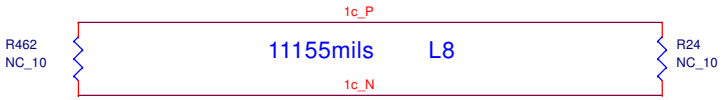
Title
144_3V3 to 3V3_I2C/FAN

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	144 of 152	015

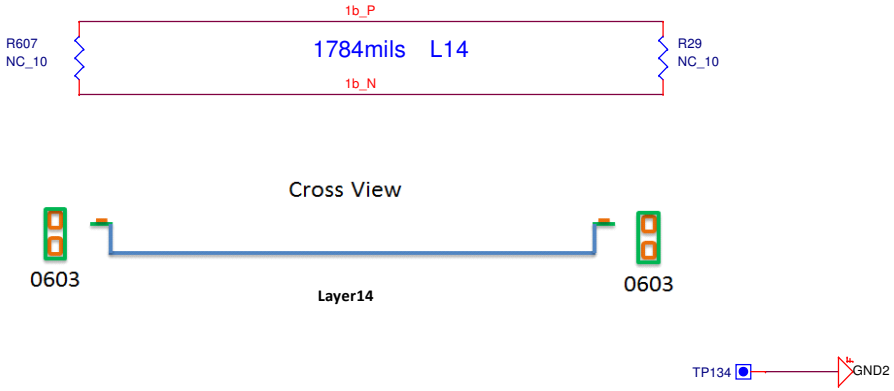
The longest trace ()



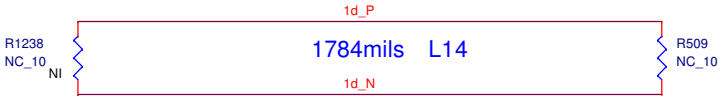
The longest trace with GND Via ()

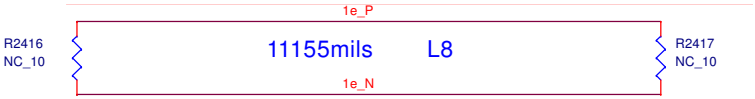


The shortest trace ()



The shortest trace with GND via()





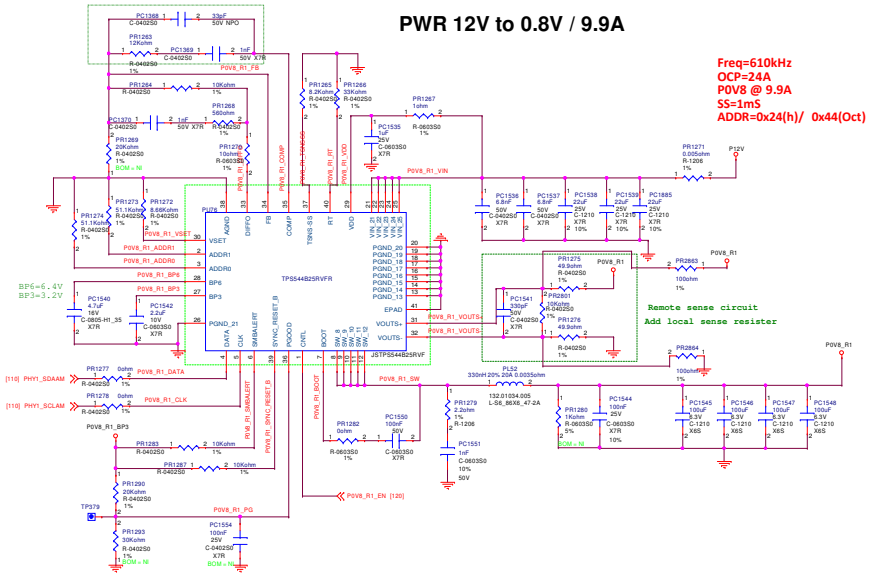
<Core Design>

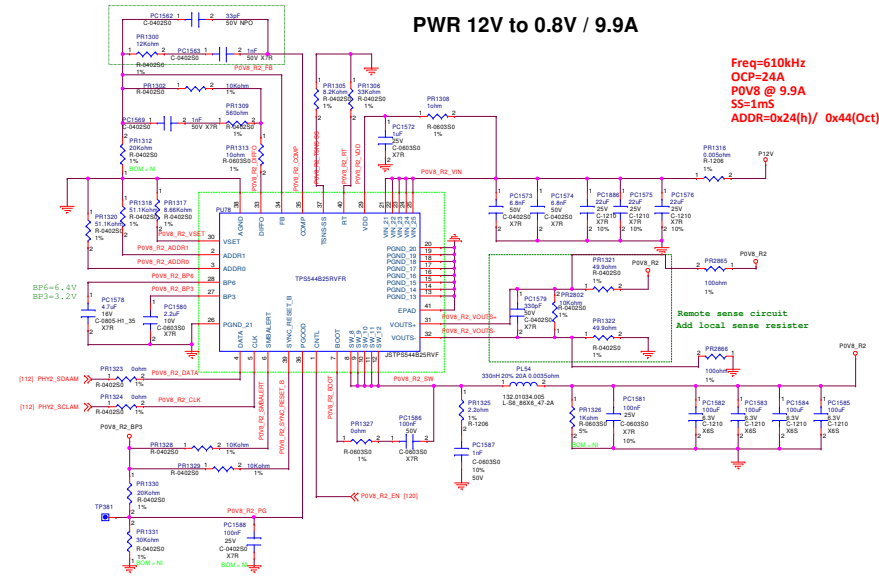
UfiSpace Co., Ltd.

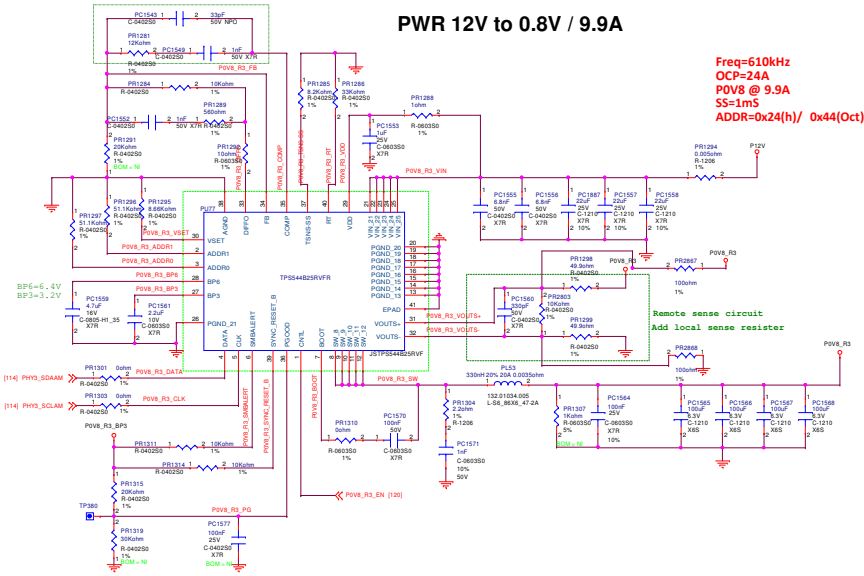
Title

145_Coupon Impendence Test

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	145 of 152	015







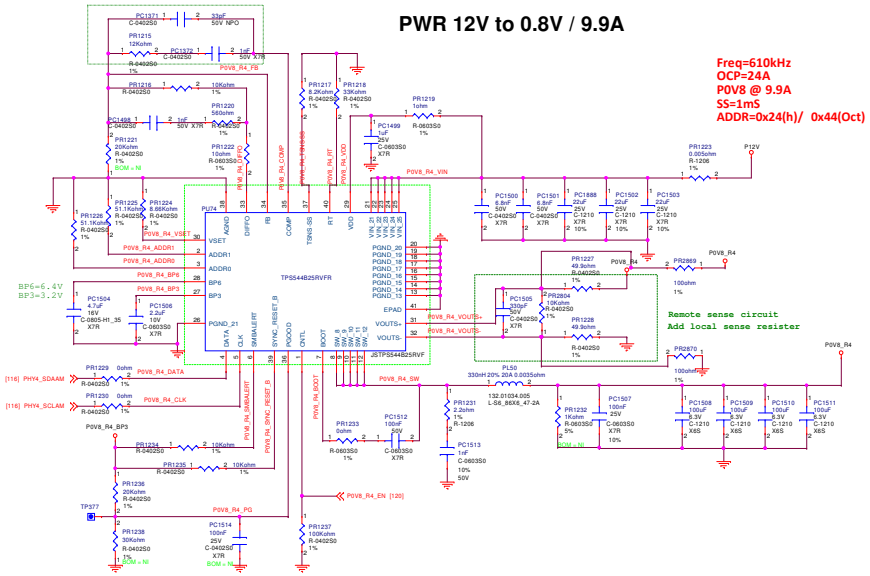
<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title: 146_12V to 0V8_Retimer/9.9A_1-3

Document Number:	Sheet	Rev
PCB P/N: T990114T00	146 of 152	015

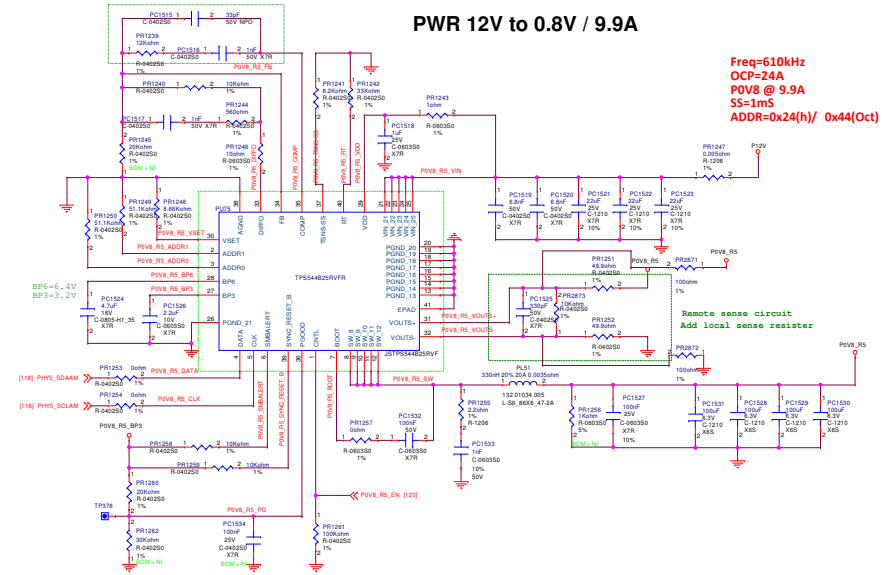
PWR 12V to 0.8V / 9.9A

Freq=610kHz
OCP=24A
P0V8 @ 9.9A
SS=1mS
ADDR=0x24(h)/ 0x44(Oct)



PWR 12V to 0.8V / 9.9A

Freq=610kHz
OCP=24A
P0V8 @ 9.9A
SS=1mS
ADDR=0x24(h)/ 0x44(Oct)



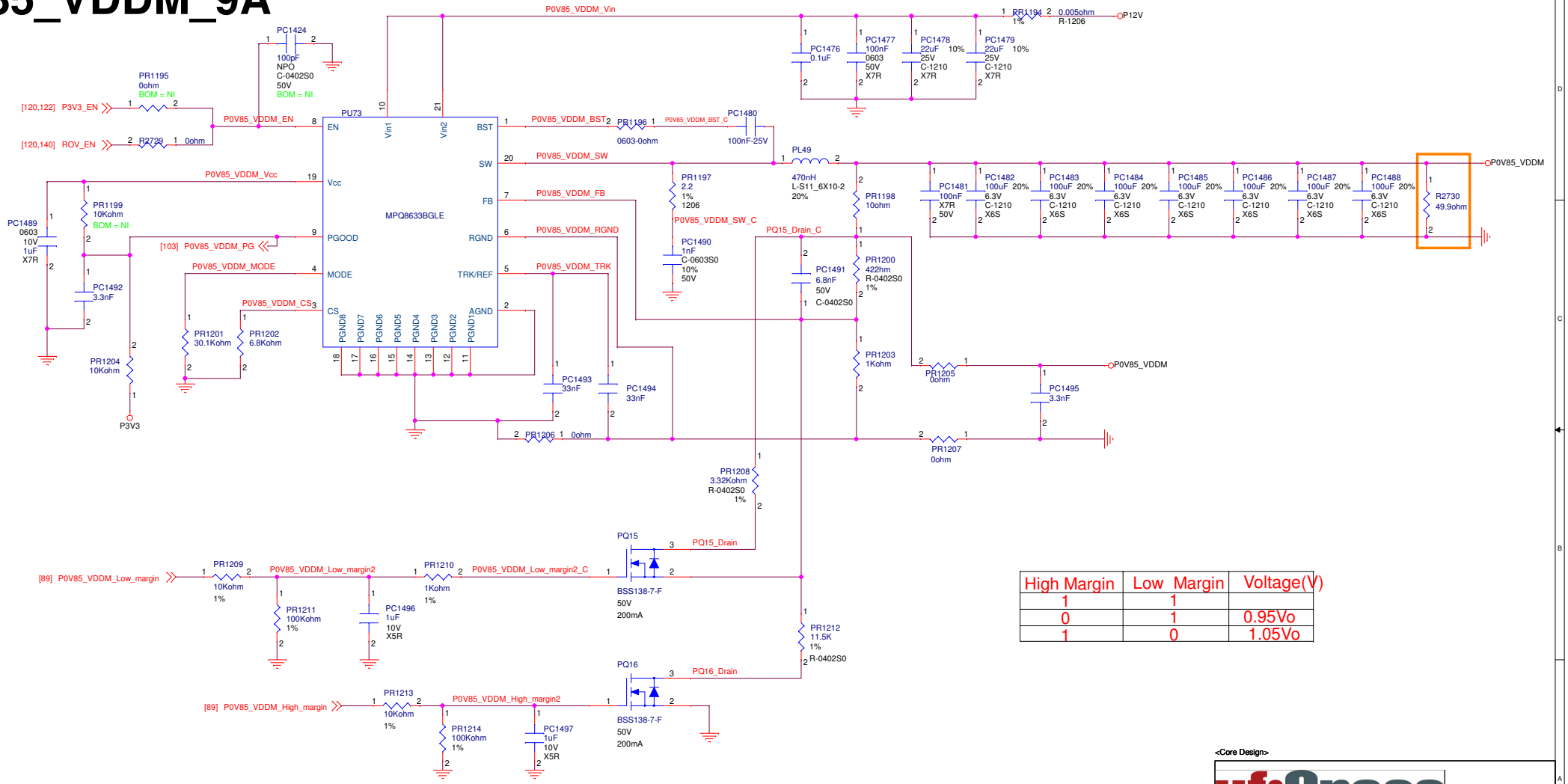
<Core Design>

ufiSpace — UfiSpace Co., Ltd.

Title: 147_12V to 0V8_Retimer/9.9A_4-5

Document Number:		Sheet	Rev
PCB P/N:	T99O114T00	147 of 152	015

P0V85_VDDM_9A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

VDDM powers the SRAM on the chip.
Its value is specified at 0.85V. A separate power supply is required for VDDM as it is a different voltage from VDD or the analog supplies.
Due to the high current requirement, a switching regulator is recommended to power VDDM.

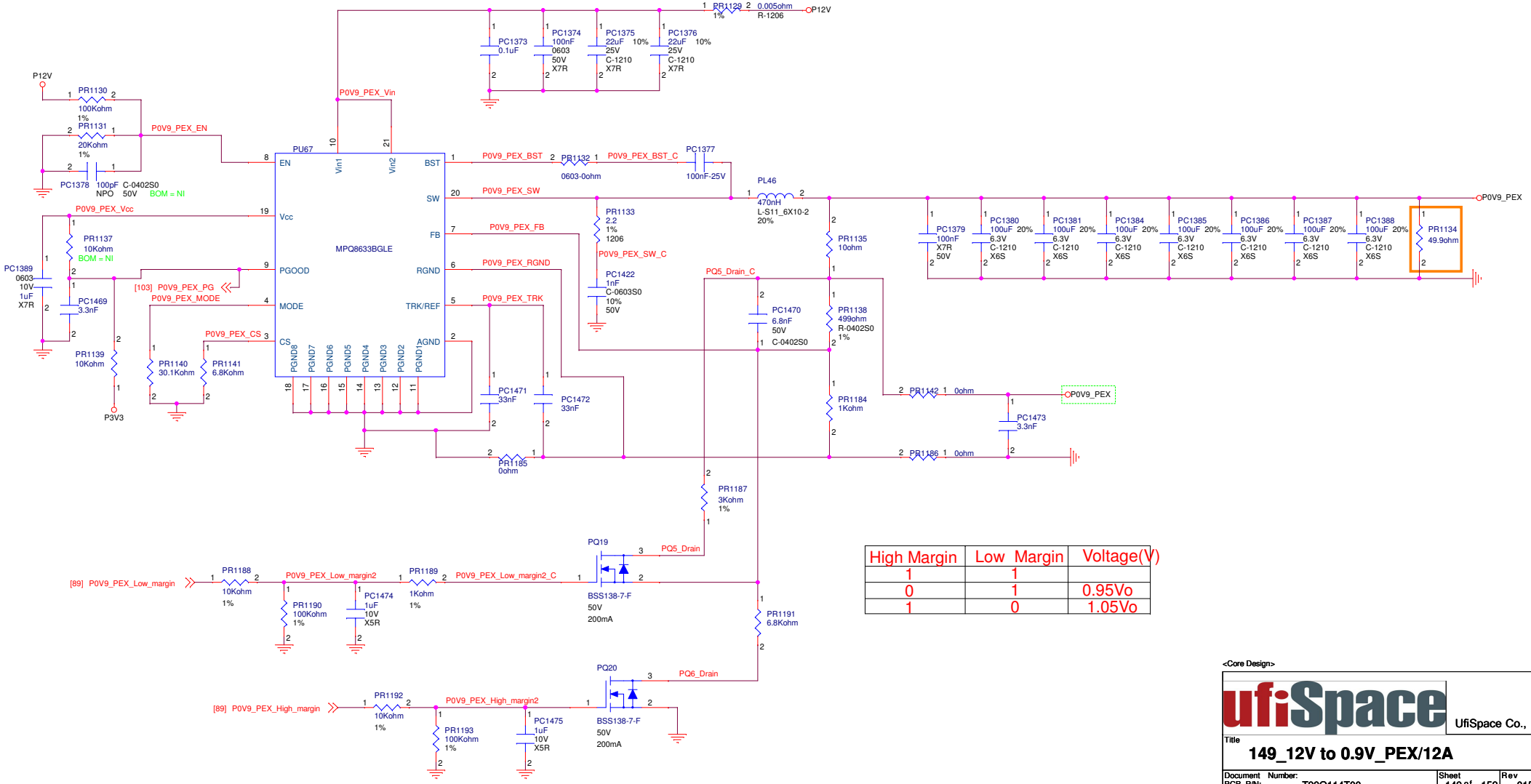
<Core Design>

UfiSpace Co., Ltd.

Title: 148_12V to 0.85V_VDDM/9A

Document Number:	PCB P/N:	Sheet	Rev
T99O114T00		148 of 152	015

P0V9_PEX_12A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

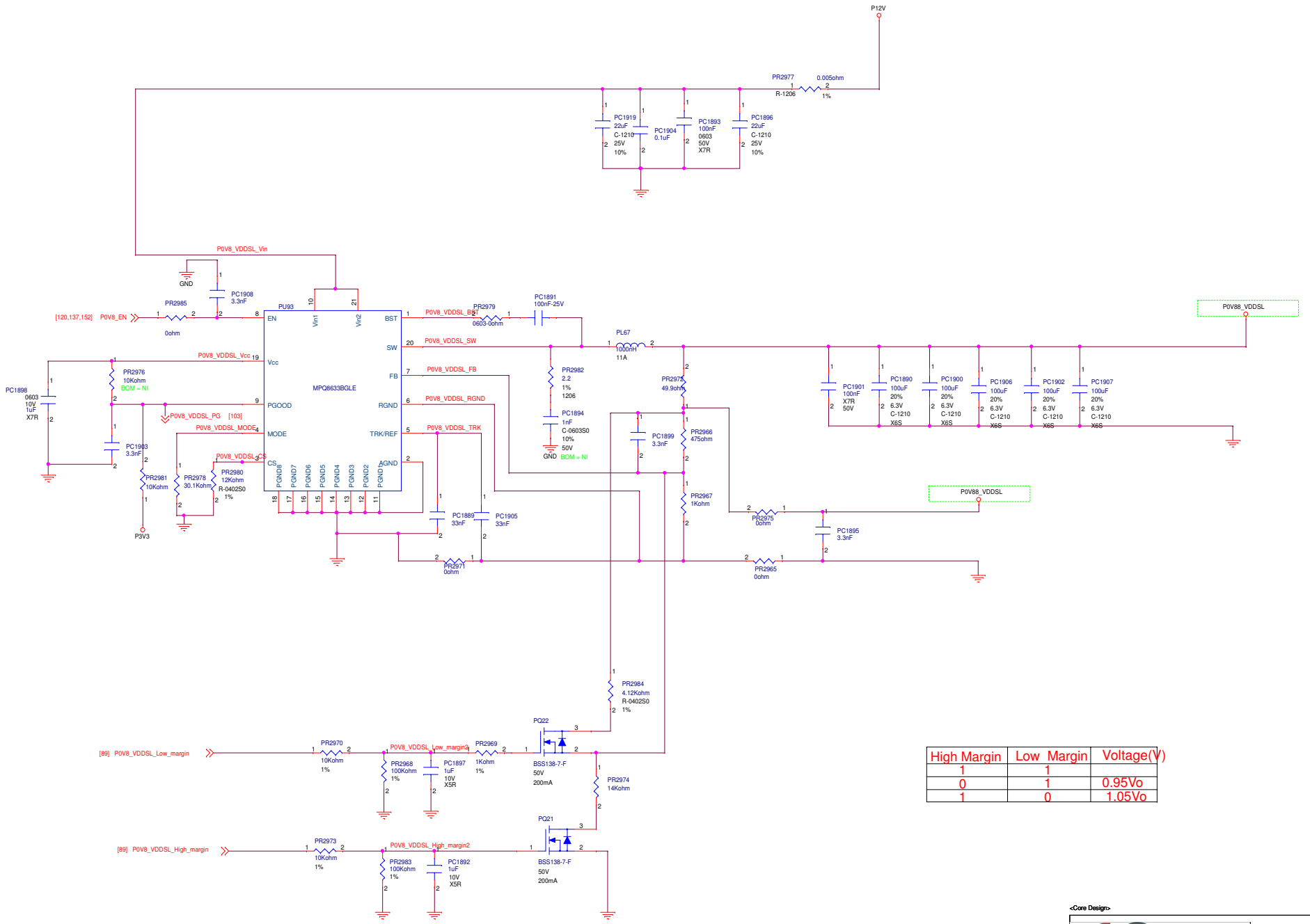
<Core Design>

UfiSpace Co., Ltd.

Title: 149_12V to 0.9V_PEX/12A

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	149 of 152	015

P0V88_VDDSL_7.5A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

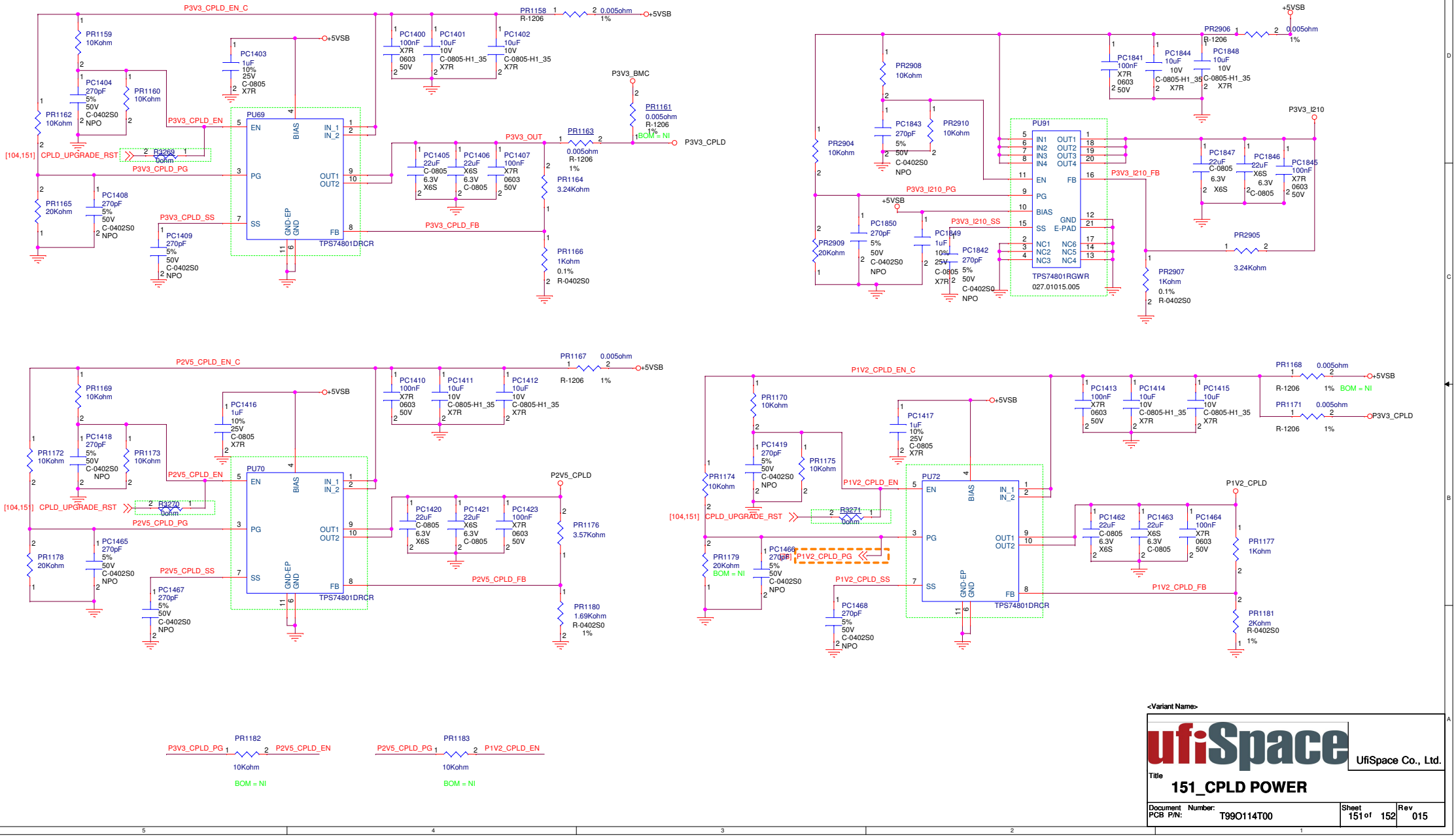
<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title: 150_3V3 to 0V8_VDDSL/0.75A

Document Number:	Sheet	Rev
PCB P/N: T99O114T00	150 of 152	015

CPLD_POWER



<Variant Name>

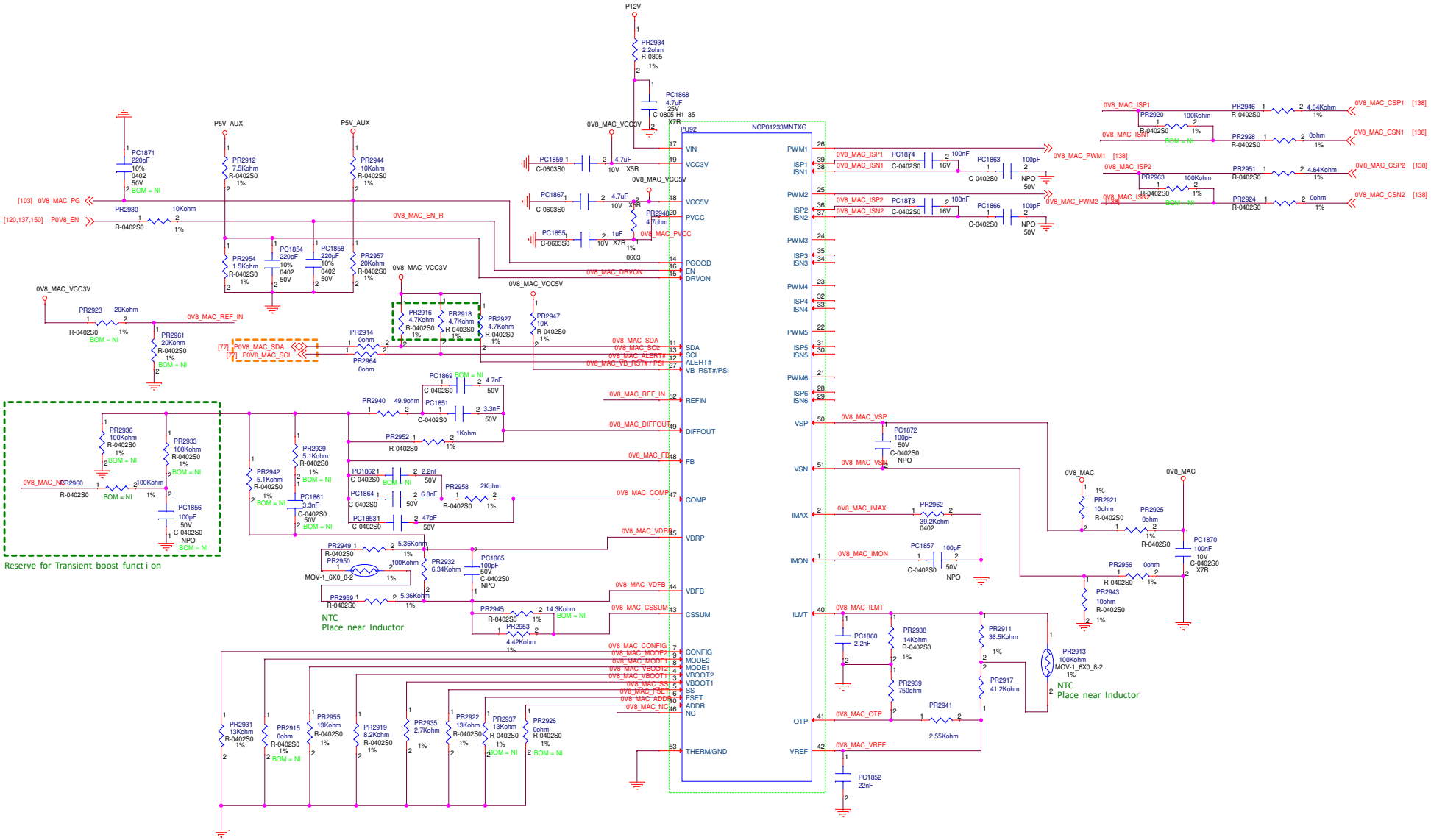
UfiSpace Co., Ltd.

Title

151_CPLD POWER

Document Number: PCB P/N:	Sheet	Rev
T99O114T00	151 of 152	015

0.80V /97A_controller
Address:0x75



CONFIG - 33k, PWM1,2,3 are active
MODE1 - 13k=> OVP,OCP,OTP,UVP/Latch Off
MODE2 - Float=> VB_RST#/ OTP1
VBOOT - 0.80V
IMAX/IMON=159.36A/2V
OCP/IMON=99.56A/1.25V
FSET - 400KHz
SS - 1mV/uS, 0.8ms Power On
ADDR -0x75